APPLICATION NOTE
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Common Issues and Solutions for SGM48211 High-Voltage Half-Bridge Gate Driver

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ABSTRACT

In low-cost applications, bootstrap power supplies are widely used to power high-voltage gate drive circuits as a replacement for isolated drivers. This approach offers simple circuitry and low cost. High-voltage half-bridge gate drivers are commonly employed in various topologies, including buck converters, synchronous boost converters, half-bridge, full-bridge, and three-phase full-bridge circuits. This application note takes the SGM48211 as an example to analyze common issues associated with high-voltage half-bridge gate driver chips and presents corresponding solutions.

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1 Introduction to Gate Drivers

A gate driver provides an interface between low-voltage control signals and high-power semiconductor switches (such as MOSFETs and IGBTs), as shown in Figure 1. It delivers the necessary voltage and current values to efficiently turn on and off power semiconductor devices.

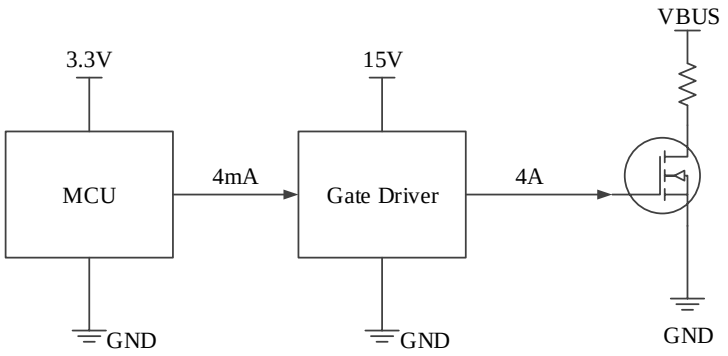


Figure 1 Driving a Power Transistor with a Gate Driver

Gate drivers feature signal amplification, isolation, and protection mechanisms. The signal amplification function boosts control signals from a microcontroller or other control circuitry, providing the required gate-source voltage (V_{GS}) for the power semiconductor device. The isolation function ensures electrical isolation between the control circuit and the power semiconductor, preventing voltage feedback or ground loop issues. Protection functions include overcurrent protection, overvoltage protection, short-circuit protection, and under voltage lockout (UVLO) to safeguard both the gate driver itself and the connected semiconductor devices. Additionally, gate drivers incorporate a dead-time control function to avoid shoot-through current. In half-bridge or full-bridge configurations, dead-time control ensures that the high-side and low-side switches are not turned on simultaneously, thus preventing device damage.

2 SGM48211 High-Voltage Half-Bridge Gate Driver

2.1 Key Advantages

The SGM48211 series 120V high-voltage half-bridge gate driver product, launched by SG Micro Corp., offers 4A source and 4A sink current capability. It can drive high-power MOSFETs with minimal switching loss. The VDD pin operates from 8V to 17V (absolute maximum 20V). The input pins withstand voltages from -10V to 20V, providing high robustness. The high-side and low-side channels are fully independent, with a propagation delay matching of 2.5ns (typical) between their turn-on and turn-off transitions. The driver includes internal UVLO protection to prevent malfunctions. The HS pin features strong immunity to negative voltage and dv/dt noise. A bootstrap diode is integrated. This device is suitable for power converters in 48V or lower voltage systems in telecommunications, data communications, and portable storage, as well as half-bridge, full-bridge, push-pull, synchronous buck, forward converters, and synchronous rectifiers.

Table 1 Key Advantages of the SGM48211

Key Advantages of the SGM48211 Driver	
HS Voltage Slew Rate: 50V/ns (MAX)	Integrated Ultra-Fast Recovery Bootstrap Diode
→ High Reliability	→ System Cost Saving (reduces PCB size and component count)

2.2 Topology

The SGM48211 integrates a high-voltage tolerant high-side driver circuit and a low-side driver circuit. The high-side driver circuit includes a high-voltage level shifter and a high-voltage floating driver. Its internal structure is shown in Figure 2, and it mainly consists of the following components:

1) Pulse Generator: generates pulse signals on the rising and falling edges of the input signal.
2) Level Shifter Circuit: converts the signal referenced to VSS to a signal referenced to HS.
3) Buffer: amplifies the input signal.
4) Bootstrap Diode: charges the bootstrap capacitor when the low-side transistor Q2 is on. Through the level shifter circuit, the HI signal referenced to ground (VSS) is converted into the HO signal synchronized and referenced to the floating ground (HS), thereby controlling the switching of the high-side transistor Q1.
5) Under voltage Lockout (UVLO) Protection: does not output a signal when the VDD voltage is below the UVLO threshold.

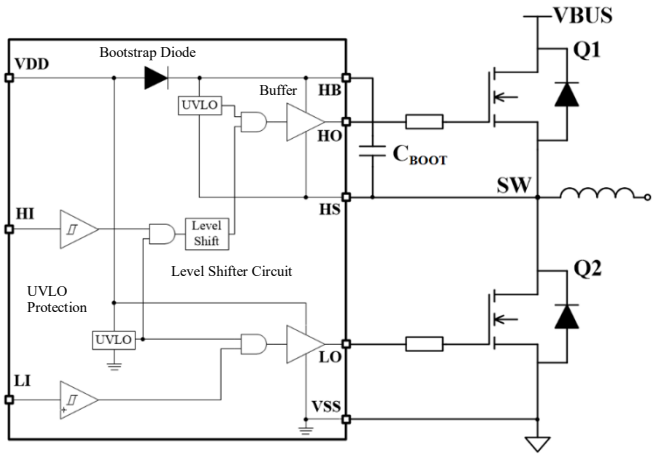
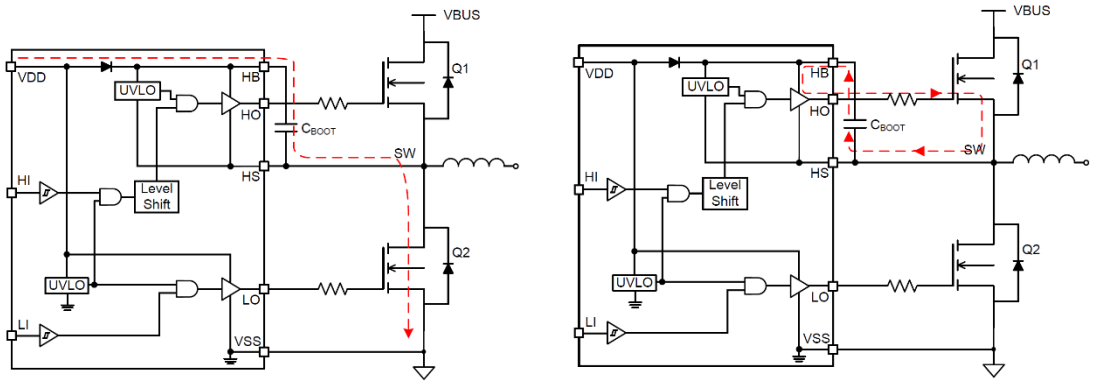


Figure 2 Topology of the High-Voltage Half-Bridge Gate Driver

2.3 Operating Principle

The SGM48211 integrates a bootstrap diode rated at 120V, which helps customers save diode circuit design effort and reduce PCB size. As shown in Figure 3, when the high-side transistor Q1 is off and the low-side transistor Q2 is on, the HS pin voltage is lower than the supply voltage VDD. VDD charges the bootstrap capacitor C_{BOOT} through the bootstrap diode D_{BOOT}, generating the V_{BS} voltage across C_{BOOT}. When Q2 is off and Q1 is on, the internal high-side MOSFET of the driver chip turns on, and the floating voltage V_{BS} across the bootstrap capacitor supports the switching of HO relative to HS. As Q1 turns on, the HS voltage becomes high, reverse-biasing the bootstrap diode, which isolates V_{BS} from the VDD supply.



(a) Q1 off, Q2 on (b) Q1 on, Q2 off

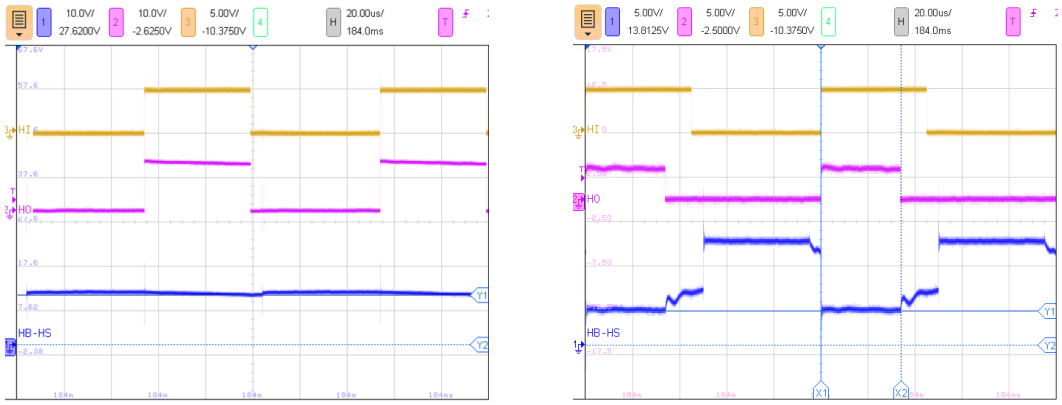
Figure 3 Operating Principle of the Bootstrap Circuit

3 Common Issues and Solutions

Next, using the SGM48211 as an example, we will explore various issues encountered when using high-voltage half-bridge gate driver products and their corresponding solutions.

3.1 Selection of the Bootstrap Capacitor C_{BOOT}

At the initial stage of circuit design, special attention must be paid to the selection of the bootstrap capacitor C_{BOOT}. It should neither be too small nor too large. When the low-side transistor Q2 is on, the HS voltage is lower than the supply voltage V_{DD}, and C_{BOOT} is charged. C_{BOOT} discharges only when the high-side transistor Q1 is on, providing the supply voltage V_{BS} to the high-side circuitry. The primary parameter to consider when selecting C_{BOOT} is the maximum allowable voltage drop across it during Q1 conduction. If the C_{BOOT} value is too small, a phenomenon as shown in Figure 4 occurs. Due to insufficient charge stored on C_{BOOT}, the V_{HB}-V_{HS} voltage drops below the UVLO threshold of the driver chip's HB pin, triggering the driver's UVLO protection. This results in no output from HO, and Q1 cannot be turned on.



(a) Appropriate C_{BOOT} (b) C_{BOOT} too small

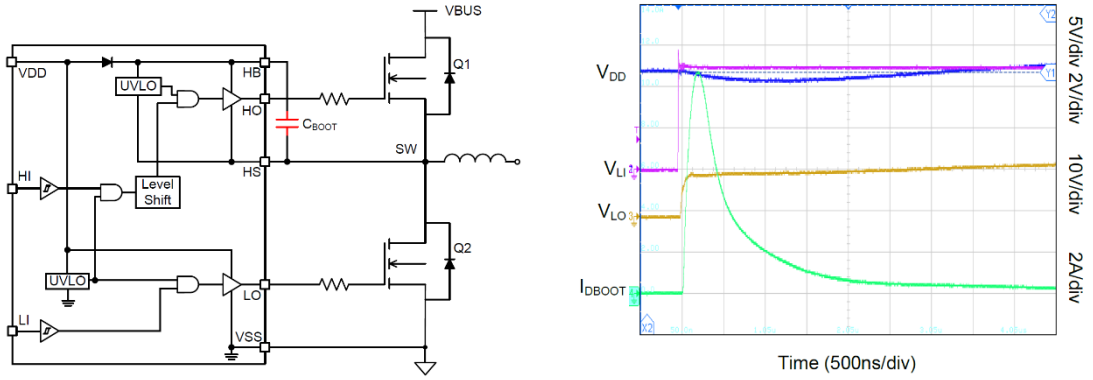
Figure 4 Impact of C_{BOOT} Value Selection

The minimum value of C_{BOOT} can be calculated using Equation (1), based on the driver chip's HB UVLO value.

$$C_{BOOT} \geq \frac{Q_{TOTAL}}{\Delta V} = \frac{Q_G + (I_{BL} + I_{RGS})t_{ON} + I_{QBS}T}{V_{DD,MIN} - V_F - V_{HB,OFF}} \quad (1)$$

Wherein, Q_G is the total gate charge of the power transistor. I_{BL} is the HB leakage current to GND. I_{RGS} is the current flowing into the gate-source resistor. I_{QBS} is the HB to HS quiescent current. t_{ON} is the high-side transistor Q1 on-time. V_F is the forward voltage drop of the bootstrap diode D_{BOOT}. $V_{HB,OFF}$ is the falling UVLO threshold of the driver chip's V_{HB}.

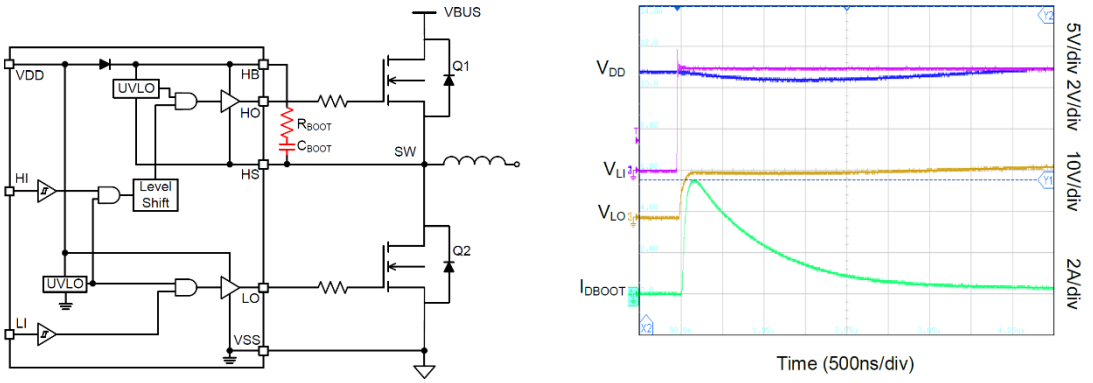
Equation (1) shows that as Q_G increases, the required C_{BOOT} value also increases. A larger C_{BOOT} leads to a higher peak charging current for the bootstrap diode. It is crucial to note that since the bootstrap diode is integrated inside the SGM48211, its die area and heat dissipation capability are limited. If the C_{BOOT} charging current exceeds the bootstrap diode's heat dissipation capability, the diode may be damaged. Figure 5 (b) shows the peak current waveform when charging the internal bootstrap diode of the SGM48211 under the condition V_{DD} = 12V: with C_{BOOT} = 680nF, the D_{BOOT} peak current is 10.7A.



(a) Without series bootstrap resistor (b) Bootstrap diode charging current

Figure 5 Bootstrap Diode Charging Current Waveform without Series Resistor for C_{BOOT}

It is evident that selecting too large a C_{BOOT} value risks damaging the bootstrap diode. In practical applications, it is recommended that C_{BOOT} does not exceed 1μF. When the MOSFET gate charge Q_G is large and C_{BOOT} must be greater than 1μF, a bootstrap resistor R_{BOOT} (typically 1Ω to 10Ω) can be connected in series with C_{BOOT} to limit the charging current, as shown in Figure 6 (a), thereby protecting the internal bootstrap diode of the SGM48211. As shown in Figure 6 (b), under conditions V_{DD} = 12V, C_{BOOT} = 680nF, and R_{BOOT} = 1Ω, the peak current capability of the SGM48211's internal bootstrap diode was tested. Compared to Figure 5 (b), the D_{BOOT} peak current was reduced from 10.7A to 5.5A.



(a) With series bootstrap resistor (b) Bootstrap diode charging current

Figure 6 Bootstrap Diode Charging Current Waveform with Series Resistor R_{BOOT} for C_{BOOT}

However, the bootstrap resistor cannot be too large, as it would increase the V_{BS} time constant. The minimum on-time of the low-side transistor Q2, which is the time available to charge or refresh the bootstrap capacitor, must match this time constant. This time constant depends on the bootstrap resistor, bootstrap capacitor, and the duty cycle of the switching device, and can be calculated using Equation (2).

$$\tau = \frac{R_{BOOT} \times C_{BOOT}}{D} \quad (2)$$

Wherein, R_{BOOT} is the bootstrap resistor. C_{BOOT} is the bootstrap capacitor. D is the duty cycle.
When a bootstrap resistor is added in series with C_{BOOT}, an additional voltage drop across this resistor must be considered:

$$V_{RBOOT} = \frac{Q_{CHARGE} \times R_{BOOT}}{t_{CHARGE}} \quad (3)$$

Wherein, Q_{CHARGE} is the total charge for charging the bootstrap capacitor. t_{CHARGE} is the charging time of the bootstrap capacitor (i.e., the on-time of low-side transistor Q2). R_{BOOT} is the bootstrap resistor.

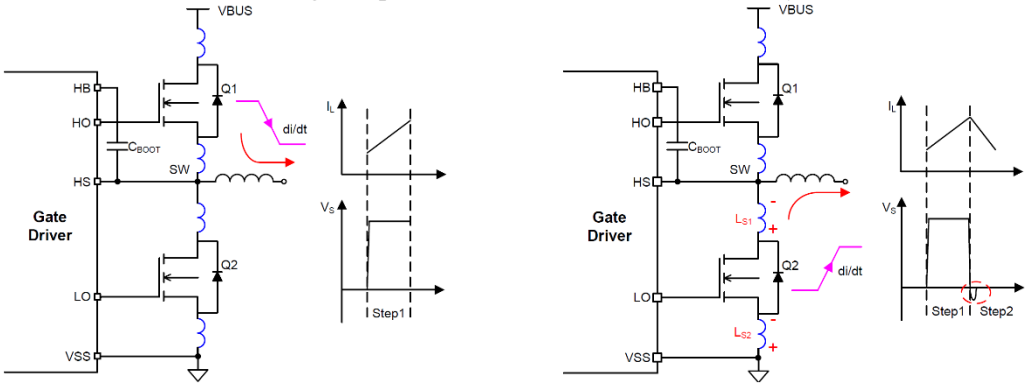
3.2 HS Pin Negative Voltage di/dt Noise

3.2.1 Causes of Negative Voltage at the HS Pin

Due to parasitic inductances from the packaging of the high-side and low-side power devices and from PCB trace routing in practical circuits, when the high-side transistor Q1 turns on, current flows through Q1 and the load inductor, as shown in Figure 7 (a). During commutation when Q1 turns off, the freewheeling current flows through the body diode of the low-side transistor Q2 and the load inductor. This current generates voltage drops across parasitic inductances like L_{S1} and L_{S2}, causing a negative voltage at the HS pin that dips below the ground voltage, as shown in Figure 7 (b). The magnitude of this negative voltage is proportional to the parasitic inductance and the current turn-off speed di/dt of the switching device, as expressed in Equation (4), where di/dt is determined by the gate drive resistor R_G and the input capacitance C_{ISS} of the switching device.

$$\begin{cases} V_{LP} = (L_{S1} + L_{S2}) \times \frac{di}{dt} \\ V_{HS} = -(V_{LP} + V_F) \end{cases} \quad (4)$$

Wherein, V_F is the forward voltage drop of the low-side transistor Q2's body diode.



(a) Q1 on, Q2 off (b) Q1 off, Q2 freewheeling

Figure 7 Application Circuit and Waveforms of the High-Voltage Half-Bridge Gate Driver

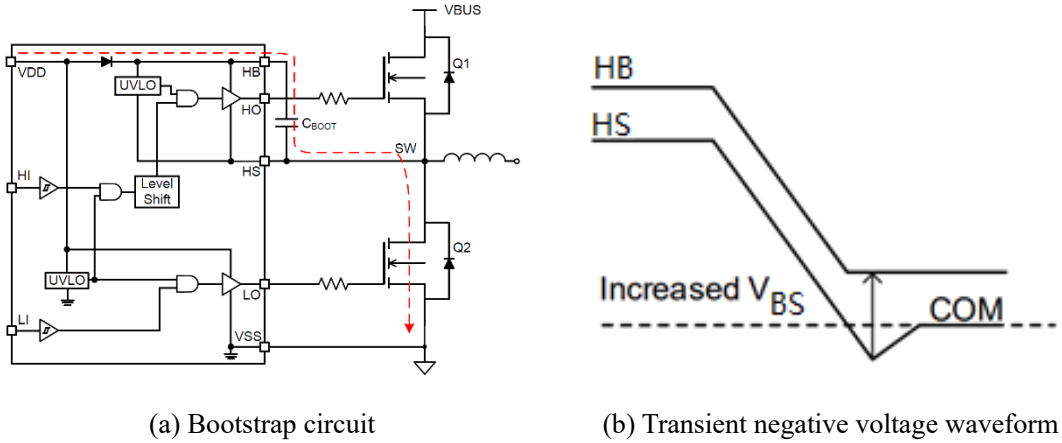
3.2.2 Effects of Negative Voltage at the HS Pin

1) Triggering Latch-up Leading to Chip Logic Abnormality:

The maximum negative voltage between HS and VSS and the recommended operating conditions are typically specified in the half-bridge driver chip datasheet. Due to internal parasitic diodes and latch-up mechanisms, excessive negative HS voltage can damage the chip or cause logic abnormalities.

2) HB-HS Overvoltage Causing Chip Damage:

The maximum voltage across the HB-HS pins is V_{HB} - V_{HS}= V_{DD} - V_F - V_{HS}. Excessive instantaneous negative voltage at the HS pin can cause the voltage across HB-HS to exceed the maximum rating, leading to overvoltage damage of the driver chip.



(a) Bootstrap circuit (b) Transient negative voltage waveform

Figure 8 Bootstrap Circuit and Transient Negative Voltage Waveforms at HB and HS Pins

3.2.3 Solutions for Negative Voltage at the HS Pin

1) Optimize Layout to Reduce Parasitic Inductance:

Place the two power transistors of the half-bridge circuit as close as possible, making the connection between them as short and wide as feasible. Place the driver chip as close as possible to the power transistors to minimize driver loop traces. Use gate drive resistors with low parasitic inductance. Use ceramic capacitors with low parasitic inductance as the bootstrap capacitor C_{BOOT}, and place C_{BOOT} as close as possible to the driver chip pins. Place decoupling capacitors as close as possible to the driver chip pins, as shown in Figure 9.

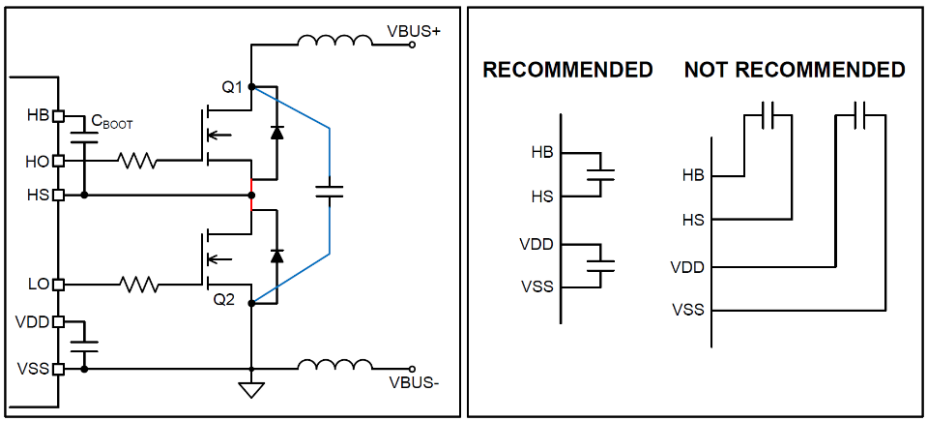


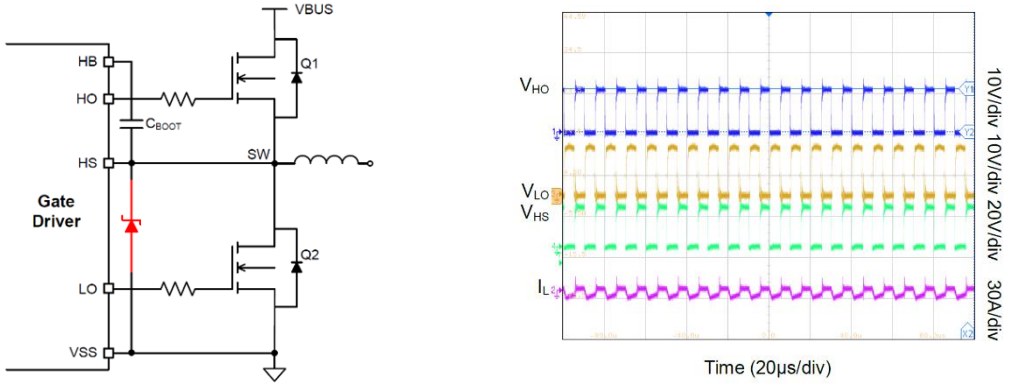
Figure 9 Layout Considerations

2) Reduce the Switching Speed of the Power Transistors:

Increase the gate drive resistance (note that this method increases power transistor switching losses) or add a snubber circuit to reduce the switching speed of the power transistors, thereby decreasing the current slew rate (di/dt) during switching.

3) Add a Schottky Diode with Low Forward Voltage Drop:

Add a Schottky diode with a low forward voltage drop between HS and VSS. This diode can quickly clamp the negative voltage at the HS pin to approximately -0.7V, as shown in Figure 10.



(a) Circuit with clamping diode (b) HS pin voltage waveform

Figure 10 Circuit with Clamping Diode and HS Pin Voltage Waveform

4) Add a Resistor in Series between HS and SW:

Connect a resistor R_{VS} in series between HS and SW, as shown in Figure 11. This resistor can reduce the negative voltage transmitted from SW to the HS pin. R_{VS} acts as a gate drive resistor, limiting the turn-on and turn-off speed of the high-side transistor Q1. It can also serve as a bootstrap resistor to limit the charging current of C_{BOOT} and limits the current through the Schottky diode during negative voltage transients at the source of Q1.

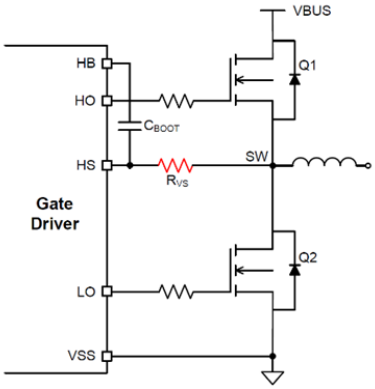


Figure 11 Circuit with Series Resistor R_{VS}

3.3 HS Pin dv/dt Noise

3.3.1 Causes of dv/dt Noise at the HS Pin

When the low-side transistor Q2 turns off and the high-side transistor Q1 turns on, current flows through Q1, the load inductor, and the capacitor. At this time, the voltage at the HS pin rises from 0V to VBUS, generating positive dv/dt noise, as illustrated in Figure 12.

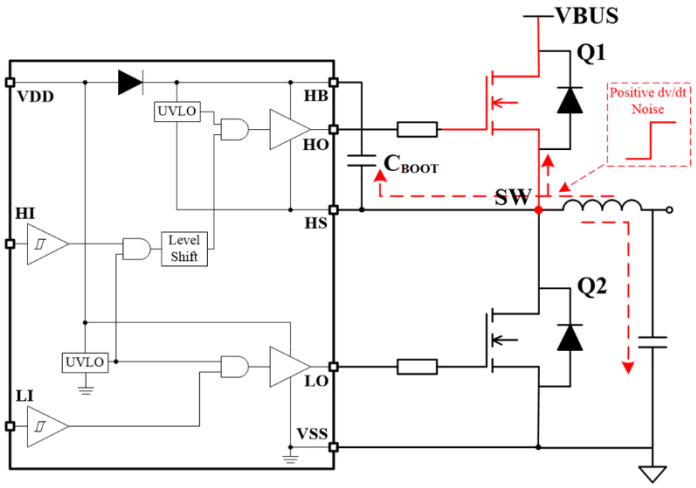


Figure 12 Positive dv/dt Noise Diagram of High-Voltage Half-Bridge Gate Driver

3.3.2 Effects of dv/dt Noise at the HS Pin

1) High-Side Circuit Logic Signal Error:

Positive dv/dt noise at the HS pin can couple to the HB node via C_{BOOT}, potentially affecting the logic signals of the high-side circuit.

2) Mistriggering of the Low-Side Power Transistor Q2:

As shown in Figure 13, when the high-side transistor Q1 is on and the low-side transistor Q2 is off, V_{DS_Q2} rises from 0V to VBUS. At this time, current i_{gd_L} flows through the parasitic capacitance C_{GD}, the gate drive resistor, and the inductance (marked by the blue dashed line). This current generates a voltage difference V_{GS_Q2} across the parasitic capacitance C_{GS}, creating a positive voltage spike that can cause Q2 to be mistakenly turned on.

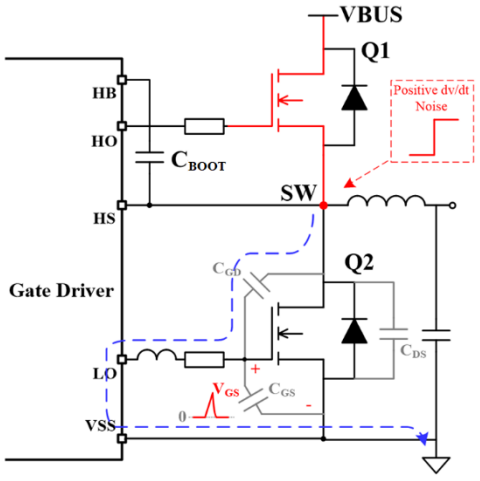


Figure 13 Impact of Positive dv/dt Noise

3.3.3 Solutions for dv/dt Noise at the HS Pin

1) Reduce Parasitic Inductance:

Keep the layout compact and use Kelvin connections. Ensure the connection between the two power transistors is as short and wide as possible. Use ceramic capacitors with low parasitic inductance.

2) Adjust the Switching Speed of the Power Transistors:

Increase the gate resistance R_{gate} of the high-side transistor Q1 to reduce its turn-on and turn-off speed, thereby decreasing dv/dt.

3) Negative Voltage Turn-Off:

Add a negative voltage drive circuit to the gate of the low-side transistor Q2, allowing Q2 to be turned off with a negative voltage. Even if a parasitic voltage is generated, it will not exceed Q2's turn-on threshold, thus preventing Q2 from being mistakenly turned on. The negative voltage drive circuit is shown in Figure 14.

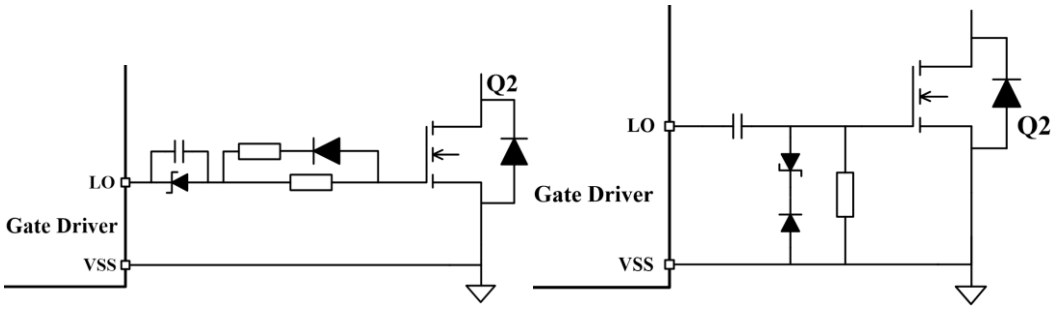


Figure 14 Negative Voltage Drive Circuit

4 Appendix

Table 2 SG Micro Corp. High-Voltage Half-Bridge Gate Driver Series

Part Number	V_{DD}, V_{HB}-V_{HS}	V_{HS}	V_{HI}, V_{LI}	t_R/t_F	Propagation Delay Time	Matching Time	Drive Peak Current (Source/Sink)	Package
SGM48211	8V~17V	-1V~105V	-10V~20V	6.6ns/4.7ns	30.5ns	2.5ns	3.7A/4.6A	SOIC-8
								SOIC-8 (EP)
								TDFN-4×4-8AL
SGM48209	8V~17V	-1V~105V	-10V~20V	6ns/4.2ns	31ns	2.5ns	3.7A/4.5A	SOIC-8
								TDFN-4×4-8AL

5 References

[1] SG Micro Corp. SGM48211 Datasheet [EB/OL]. (2026-01). https://www.sg-micro.com/rect/assets/aafd63b4-ebd1-47cd-903f-9182d2e58852/SGM48211.pdf.

[2] Design and Application Guide for High-Voltage Gate Driver IC Bootstrap Circuits [EB]. (2022-12-13).

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from those in the current version.

Date	Rev	Description
2026-05-26	REV.A	Initial Release

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