APPLICATION NOTE
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Reconfiguring SGM61630 Series Buck Converter as an Inverting Buck-Boost Converter

Author: Kai Deng
Corresponding Author: Cherry Cheng
Reviewers: Hui Liu, Jason Liu

SG Micro Corp

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ABSTRACT

This document takes the SGM61630 as an example to systematically present the design methodology for reconfiguring a Buck converter into an inverting Buck-Boost converter to generate a stable negative power rail. The design procedure is elaborated through topology connection adjustment, voltage and current stress analysis, and auxiliary function design. Finally, a design example verifies the feasibility of achieving a -15 V/1.5 A output from a 24 V input. This document provides engineers with a complete design workflow from theoretical derivation to practical validation.

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1 Introduction

Many precision systems (such as medical electronic equipment and test and measurement instruments) require a stable negative voltage supply while also requiring the input and output to share a common ground. An inverting Buck-Boost converter perfectly meets this requirement, as it not only achieves step-up/step-down functionality but also inverts the output voltage polarity. By adjusting the power stage topology connection and feedback network parameters, any conventional Buck converter can be reconfigured as an inverting Buck-Boost converter. This document takes the SGM61630 as an example to elaborate on its reconfiguration method and design considerations. This approach is applicable to the implementation of inverting Buck-Boost converters in both synchronous rectification and non-synchronous rectification architectures.

2 Inverting Buck-Boost Converter Principle

2.1 Topology Reconfiguration and Connection Method

Figure 1 shows the basic topology of a Buck converter. In the Buck configuration, the output positive terminal (V_{OUT}) is connected to the inductor, while the output negative terminal is connected to the GND pin of the Buck IC.

The inverting Buck-Boost topology is very similar to the Buck topology. Figure 2 shows the connection method for reconfiguring a Buck converter as an inverting Buck-Boost converter. As shown in Figure 2, the positive output terminal of the Buck converter is configured as the system ground (System GND) of the inverting Buck-Boost converter, while "IC GND" becomes the negative output terminal ($-V_{OUT}$). An additional input capacitor C_{IN} is added between the input power supply and the system ground. It should be noted that in the connection method of the inverting Buck-Boost converter, IC GND is directly connected to the negative output voltage, which affects the voltage stress on the pins of the Buck IC. The external circuits for the relevant control pins must be redesigned, as detailed in the "3 Auxiliary Function" section.

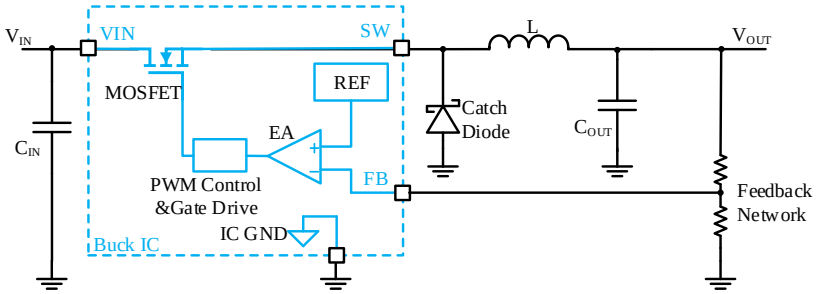


Figure 1 Basic Buck Converter Topology

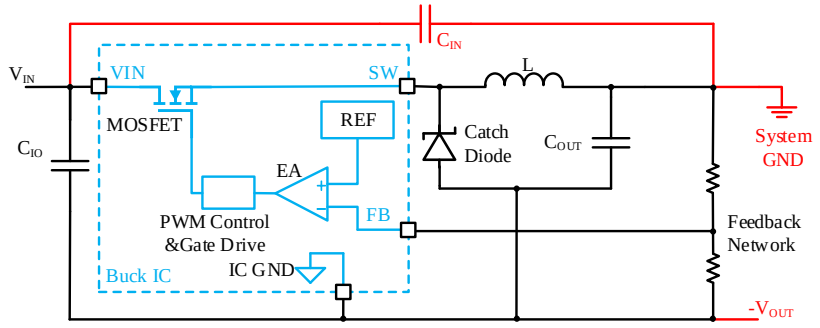
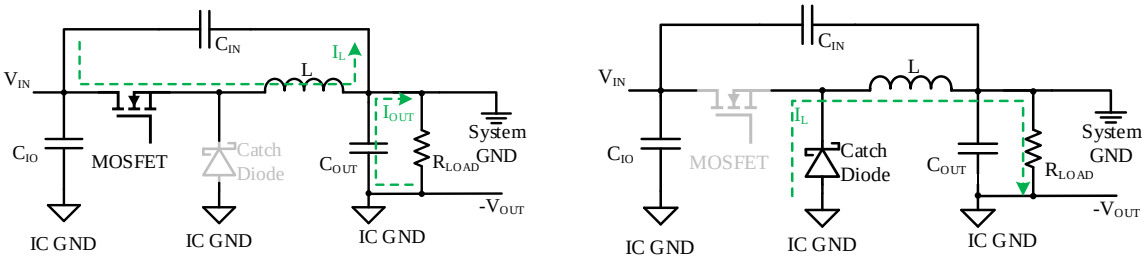


Figure 2 Inverting Buck-Boost Converter Topology

After the above steps, the reconfiguration of the inverting Buck-Boost converter is achieved: when the MOSFET is turned on, the power diode is reverse-biased, the voltage across the inductor is V_{IN}, the inductor current rises, and the output capacitor C_{OUT} supplies energy to the load, as shown in Figure 3 (a); when the MOSFET is turned off, the power diode conducts, the voltage across the inductor is $-V_{OUT}$, the inductor current decreases, and the inductor current supplies energy to the load, as shown in Figure 3 (b). The duty cycle D in continuous conduction mode (CCM) is given by:

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}} \quad (1)$$



(a) MOSFET ON (b) MOSFET OFF

Figure 3 Inverting Buck-Boost Converter Principle

2.2 Voltage and Current Stress Analysis

Configuring a Buck IC as an inverting Buck-Boost converter requires special attention to voltage requirements. From Figure 2, it can be seen that the voltage difference between the VIN and GND pins of the Buck IC equals the input voltage plus the output voltage ($V_{MAX}=V_{IN}+V_{OUT}$) of the power module. For example, for a conversion from a +24 V input to a -15 V output, a Buck IC with an input voltage range covering at least 39 V is required. When the MOSFET is turned on, the voltage stress across the power diode is also the input voltage plus the output voltage ($V_{MAX}=V_{IN}+V_{OUT}$), which should be considered when selecting the power diode.

As shown in Figure 2, the capacitor C_{IO} connected between V_{IN} and $-V_{OUT}$ also withstands a voltage stress of ($V_{IN}+V_{OUT}$). However, it is worth noting that if V_{IN} is powered up quickly, a transient current is generated at the moment of power-up. Its path is: V_{IN} → C_{IO} → IC GND → power diode → inductor → System GND. This transient current may have the following effects on the circuit: (1) When the transient current flows through the power diode (or the body diode of a synchronous Buck IC), the SW node potential may be pulled below IC GND. For devices with a small rated voltage of SW relative to IC GND, such negative voltage transients may damage the device; (2) The transient current flowing through the power inductor generates an induced electromotive force. The combined effect of the diode and the induced electromotive force results in a transient positive voltage on V_{OUT}. Therefore, based on the trade-off between protecting against the transient voltages mentioned above and decoupling the Buck IC VIN pin, it is recommended that the C_{IO} capacitor not be too large; a value of 0.1 μF is generally recommended.

In the Buck converter configuration, the inductor always supplies current to the load during both the MOSFET on-time and off-time, so the average inductor current of the Buck converter equals the output current. However, in the inverting Buck-Boost converter configuration, the energy in the inductor is delivered to the load only during the MOSFET off-time via the diode. The inductor current calculation formulas for the two topologies are shown in Table 1.

Table 1 Comparison of Inductor Current in Buck Topology and Buck-Boost Topology

Topology	Duty Cycle	Average Inductor Current	Inductor Peak Current
Buck	$D = \frac{V_{OUT}}{V_{IN}}$	$I_{L(avg)} = I_{OUT}$	$I_{L(peak)} = I_{OUT} + \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_{SW}}$
Buck-Boost	$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}}$	$I_{L(avg)} = \frac{I_{OUT}}{1 - D}$	$I_{L(peak)} = \frac{I_{OUT}}{1 - D} + \frac{D \times V_{IN}}{2 \times L \times F_{SW}}$

As can be seen from Table 1, under the same load, the inductor peak current of the inverting Buck-Boost converter is larger. During reconfiguration, care must be taken to ensure that the inductor peak current does not exceed the peak current limit specified in the Buck IC datasheet.

For specific calculations using the SGM61630 as an example, please refer to the "4 Design Example" section.

3 Auxiliary Function

In the inverting Buck-Boost converter configuration, IC GND is directly connected to the negative output voltage. Since all control signal levels of the Buck IC are referenced to IC GND, if these functions need to be used in the system, the reference level of the control signals must be shifted to the system ground.

3.1 Enable Signal Interface Design

If the system is not required to control enable signal, the EN pin can be pulled up to V_{IN} through a resistor. If the system is required to control the enable function of the inverting Buck-Boost converter, a simple level-shifting circuit is needed, as shown in Figure 4.

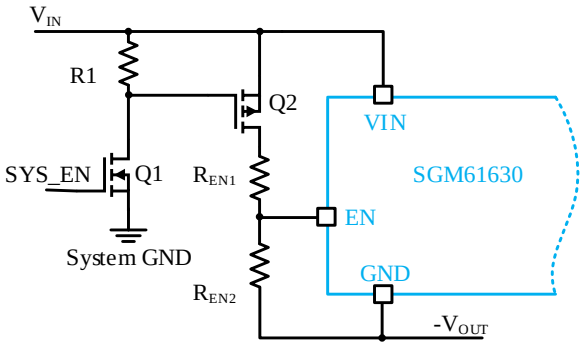
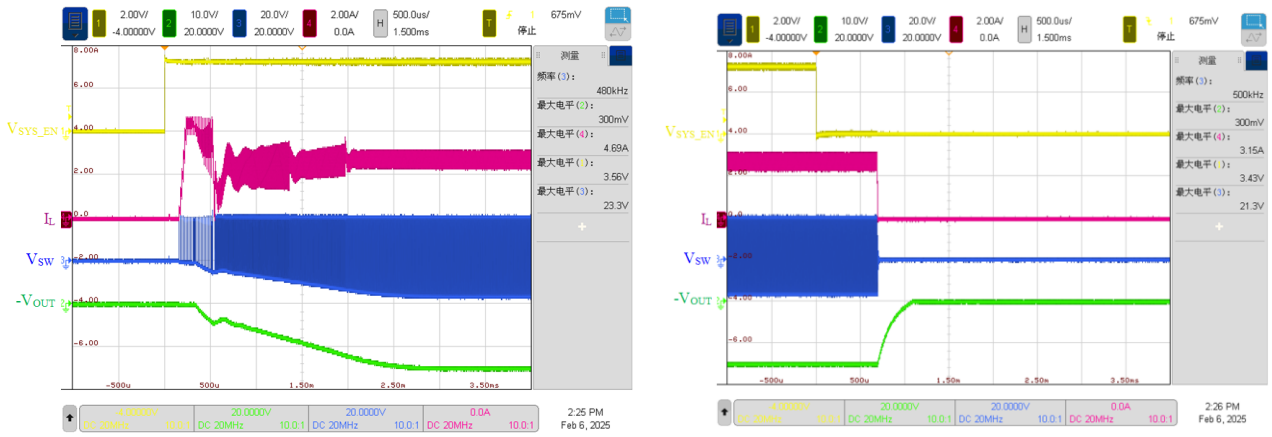


Figure 4 EN Level Shifting Circuit

When SYS_EN provides a sufficiently high positive voltage to turn on Q1, the gate of Q2 is connected to ground through Q1, making the gate-source voltage (V_{GS}) of Q2 negative, thereby turning on Q2. At this time, the input voltage (V_{IN}) is connected to the EN pin through the resistor divider, enabling the device. It should be noted that in both the enable and disable states, the gate-drain voltage (V_{GD}) and gate-source voltage (V_{GS}) of Q2 must remain within the MOSFET's rated range. Taking the SGM61630 as an example, set R_{EN1} = R_{EN2} = R1 = 100kΩ in Figure 4. Figure 5 shows the waveforms for system-controlled enabling and disabling of the inverting buck-boost converter, tested under conditions of 20 V input and -15 V/1.5 A output.



(a) EN On (b) EN Off

Figure 5 Inverting Buck-Boost Converter Enable and Disable Waveforms

If it is required to use the EN pin to configure the UVLO (Under-Voltage Lockout) of the inverting Buck-Boost converter, a resistor divider can be set at the EN pin as shown in Figure 6.

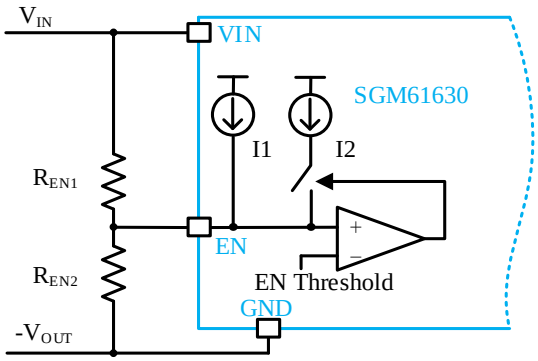


Figure 6 EN Voltage Divider Circuit

The turn-on voltage V_{START} remains unchanged because there is typically no negative output voltage when the inverting Buck-Boost converter starts up.

$$V_{START} = V_{ENH} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}} - I1 \times R_{EN1} \quad (2)$$

After the inverting Buck-Boost converter starts up, the turn-off voltage V_{STOP} needs to account for the negative output voltage:

$$V_{STOP} = V_{ENL} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}} - (I1 + I2) \times R_{EN1} - V_{OUT} \quad (3)$$

Taking the SGM61630 as an example, V_{ENH} = 1.17V, V_{ENL} = 1.12V. Set R_{EN1} = 430kΩ, R_{EN2} = 30kΩ, I1 = 1μA, I2 = 3.7μA, $-V_{OUT}$ = -15 V. Then the turn-on voltage V_{START} is 17.51 V, and the turn-off voltage V_{STOP} is 0.15 V.

3.2 Synchronization Signal Interface Design

For Buck IC with a SYNC input pin, if the inverting Buck-Boost converter is required to synchronize with an external signal, a simple level shifter is needed, as shown in Figure 7.

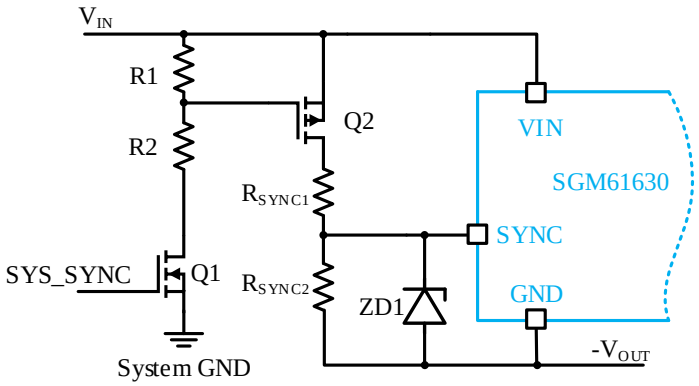


Figure 7 Synchronization Signal Level Shifting Circuit

When SYS_SYNC is high, Q1 turns on, V_{IN} provides the drive voltage V_{GS} to Q2 through the resistor divider (R1, R2), Q2 turns on, and V_{IN} pulls the SYNC pin high through the resistor divider (R_{SYNC1}, R_{SYNC2}). Note that the maximum rated voltage of the SYNC pin is typically low, so a Zener diode ZD1 is required to protect the chip from damage. Considering power dissipation, the resistance of the resistor divider from V_{IN} to System GND should not be too small. Therefore, in scenarios with high synchronization frequencies, a P-MOSFET with a small gate charge Q_G should be selected for Q2.

When SYS_SYNC is low, Q1 turns off, then Q2 turns off. After Q2 turns off, the SYNC pin is pulled down to $-V_{OUT}$ through R_{SYNC2}. Due to the junction capacitance C_j of the Zener diode ZD1, there will be an additional delay t_{delay} between the valid synchronization signal and the rising edge of SW (this delay does not include the internal circuit delay of the chip).

Taking the SGM61630 as an example, set R1 = 499 Ω, R2 = 1 kΩ, R_{SYNC1} = 1kΩ, R_{SYNC2} = 200Ω in Figure 7. The synchronization mechanism of this Buck IC is that the rising edge of SW synchronizes with the falling edge of SYNC. The falling edge of SYS_SYNC turns off Q2. After Q2 turns off, C_j discharges through R_{SYNC2}. When the voltage at the SYNC pin discharges from the Zener voltage V_Z of ZD1 to the SYNC pin low threshold V_{SYNC_L}, the power switch turns on. This causes the rising edge of SW to lag behind the falling edge of SYS_SYNC. The delay time is:

$$t_{delay} = R_{SYNC2} \times C_j \times \ln \frac{V_{SYNC_L}}{V_Z} \quad (4)$$

From the above equation, it can be seen that for high-frequency synchronization requirements, a Zener diode with a smaller junction capacitance should be selected. The synchronization waveforms of the SGM61630 is shown in Figure 8.

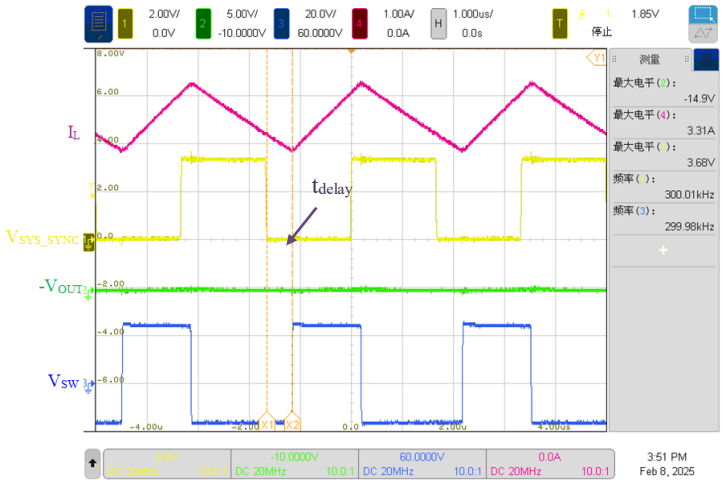


Figure 8 Synchronization Waveforms

3.3 PG Signal Interface Design

If the system does not require the Power Good (PG) flag signal from the inverting Buck-Boost converter, the PG pin can be left floating. If the system needs to obtain the PG signal to indicate to the MCU that the output voltage is within the specified range, the PG flag signal needs to be level-shifted to the system ground. The shifting circuit is shown in Figure 9.

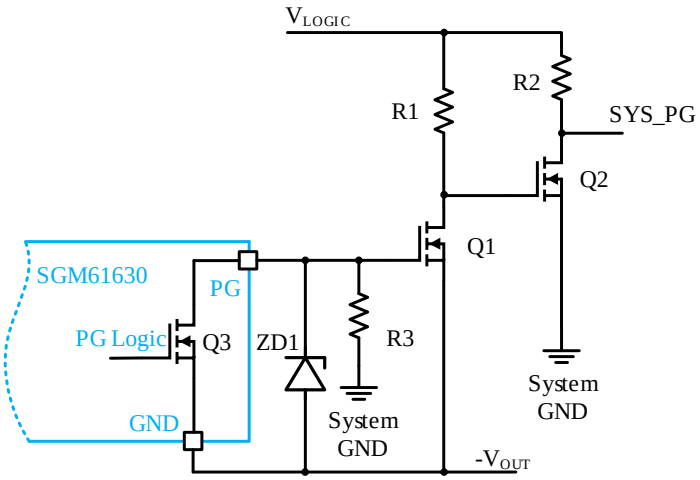
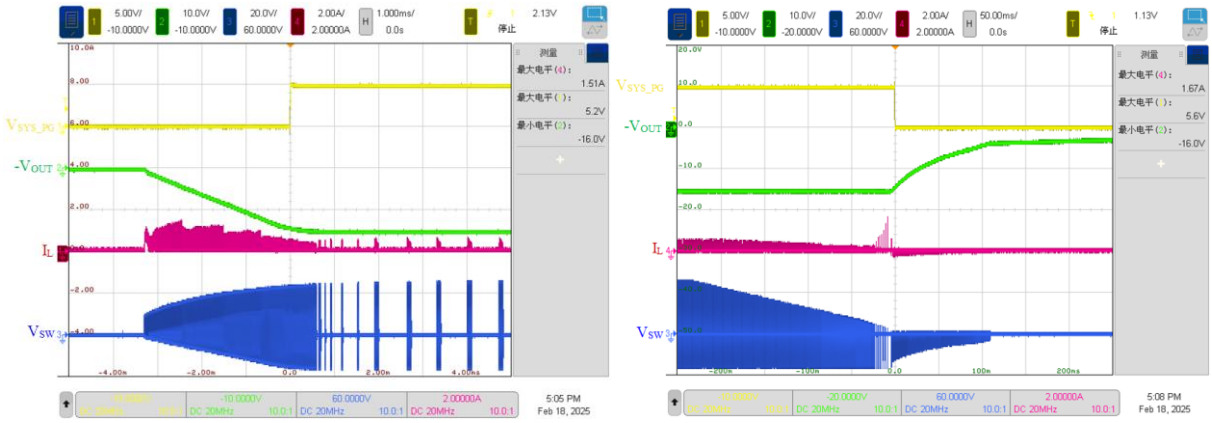


Figure 9 PG Level Shifting Circuit

When the output voltage is not fully established, the internal Q3 of the chip is turned on, and PG is pulled down to $-V_{OUT}$. At this time, Q1 is off and Q2 is on, and SYS_PG is pulled down to system ground. When the output voltage is fully established, Q3 turns off, and PG is pulled up to $(-V_{OUT}+V_Z)$. At this time, Q1 turns on, and the gate-source voltage of Q2 becomes negative, turning it off, and SYS_PG is pulled up to the logic level V_{LOGIC}. Note that if the maximum rated voltage of the PG pin is relatively low and V_{OUT} is large, a Zener diode ZD1 should be added to protect the chip from damage.

Taking the SGM61630 as an example, set R1 = R2 = 100 kΩ, R3 = 10 kΩ in Figure 9. Figure 10 shows the waveforms of SYS_PG during Power-on and Power-off of the inverting Buck-Boost converter, tested under conditions of 24 V input and -15 V/0 A output.



(a) Power On (b) Power Off

Figure 10 Inverting Buck-Boost Converter Power-on and Power-off Waveforms

4 Design Example

This chapter will design an inverting Buck-Boost converter based on the SGM61630 Demo Board (Buck)[1]. The design targets are shown in Table 2.

Table 2 Design Targets

Input Voltage (V_{IN})	Output Voltage (-V_{OUT})	Output Current (I_{OUT})	Switching Frequency (F_{SW})
24V	-15V	1.5A	490kHz

4.1 Schematic

The schematic of the inverting Buck-Boost converter is shown in Figure 11.

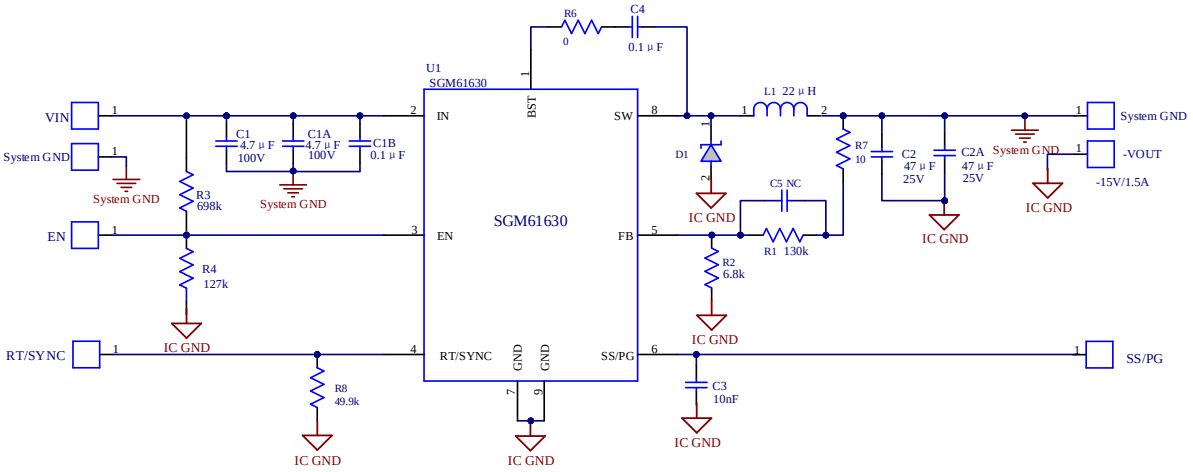


Figure 11 Inverting Buck-Boost Converter Schematic

To preliminarily verify the feasibility of this solution, the connection method can be directly modified on the SGM61630 Demo Board in Buck topology to reconfigure it into an inverting Buck-Boost topology, as shown in Figure 12. For actual new projects, it is necessary to re-layout the PCB according to the layout considerations for Buck-Boost converters to achieve optimal performance.

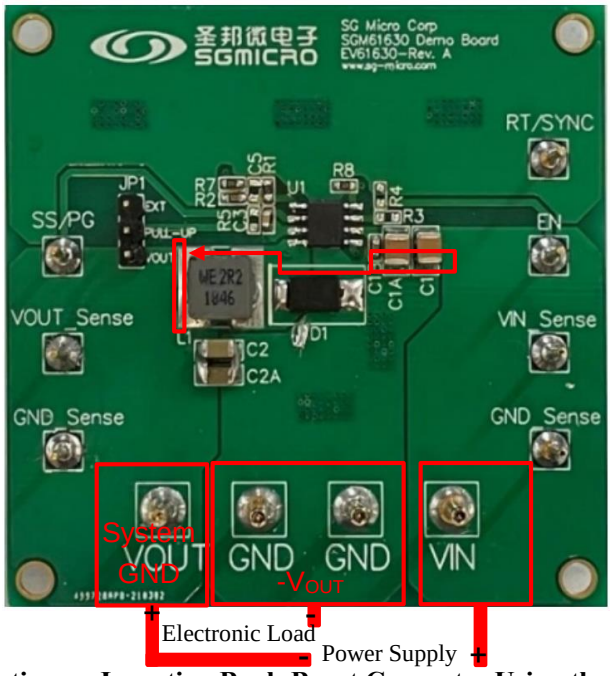


Figure 12 Constructing an Inverting Buck-Boost Converter Using the Buck Demo Board

Notes:

1) Disconnect the lower-side connection of the original input capacitors C1, C1A, and C1B from IC GND, and reconnect them to the left pad of L1 (System GND). The reconnection wires should be as short as possible to minimize the impact of parasitic inductance on the input voltage.
2) Connect a 24 V power supply between "VIN" and "VOUT" on the Demo Board; connect an electronic load between "VOUT" and "GND" on the Demo Board.
3) Replace the inductor with a 22 μH inductor.

4.2 Key Parameter Calculation

The duty cycle of the inverting Buck-Boost converter is:

$$D = \frac{V_{OUT}}{V_{OUT} + V_{IN}} = 0.38 \quad (5)$$

To facilitate the evaluation of the voltage withstand capability of the chip's VIN and SW pins, as well as the selection of related peripheral components, the voltage stress V_{MAX} of the Buck regulator is calculated as $V_{MAX} = V_{IN} + V_{OUT} = 39V$.

To balance inductor size and converter efficiency, select an inductor current ripple ratio of 0.35. The inductance value is then:

$$L = \frac{D \times (1 - D) \times V_{IN}}{0.35 \times I_{OUT} \times F_{SW}} = 21.9\mu H \quad (6)$$

In this design example, L = 22 μH is selected. The inductor peak current is:

$$I_{L(peak)} = \frac{I_{OUT}}{1 - D} + \frac{D \times V_{IN}}{2 \times L \times F_{SW}} = 2.83A \quad (7)$$

This is less than the minimum value of I_{LIMT} (3.5 A) specified in the SGM61630 datasheet[2].

The inverting Buck-Boost converter has a right-half-plane zero (RHPZ), which increases gain and reduces phase at high frequencies, significantly and negatively impacting the control loop response and potentially causing system instability. The right-half-plane zero frequency for this design example under full load (worst-case condition) is:

$$F_{RHPZ} = \frac{R_L \times (1-D)^2}{2 \times \pi \times D \times L} = 73kHz \quad (8)$$

To ensure sufficient phase margin and system stability, it is generally recommended to set the system's crossover frequency to less than 1/4 of the RHPZ frequency. Therefore, it is necessary to reduce the inductance to increase the RHPZ frequency, or increase the output capacitance to reduce the system's crossover frequency. It is particularly important to note that in the inverting Buck-Boost converter architecture, the feedforward capacitor in the phase compensation network should be added with caution. Although the feedforward capacitor can improve phase margin, it simultaneously causes the gain curve in the magnitude-frequency characteristic to shift upward, which will cause the crossover frequency to move toward the RHPZ frequency, thereby introducing potential system stability risks.

To ensure that the system's crossover frequency is less than 1/4 of the RHPZ frequency, in this design example, two 47 μF / 25 V X5R capacitors in parallel are used for C_{OUT}.

4.3 Test Results

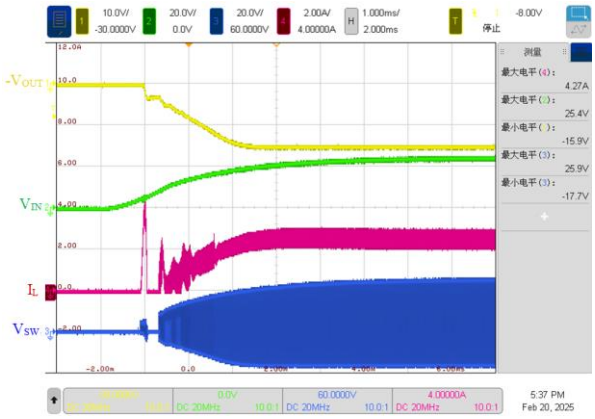


Figure 13 V_{IN} = 24V, -15V/1.5A Output, Power On

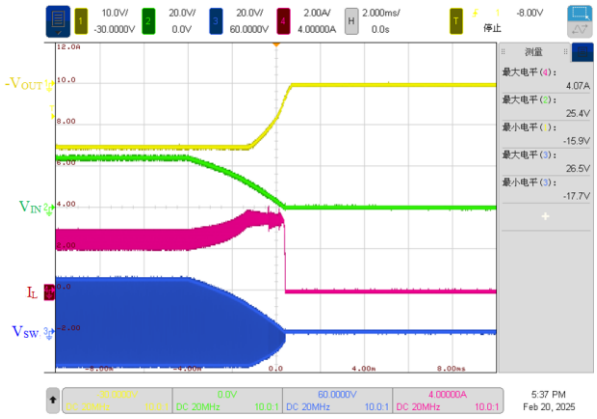


Figure 14 V_{IN} = 24V, -15V/1.5A Output, Power Off

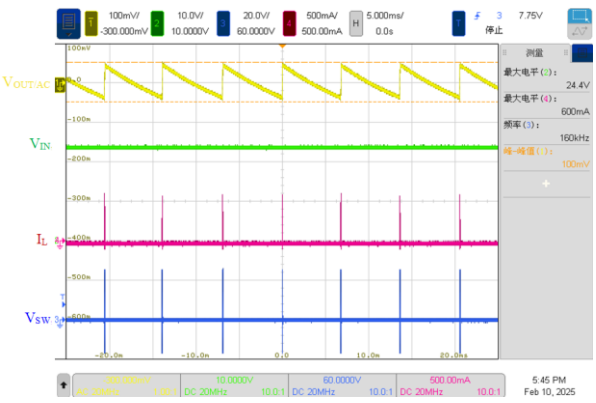


Figure 15 24V Input, -15V/0A Output

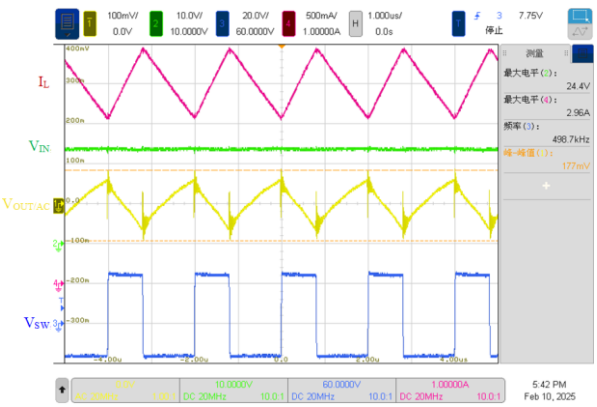


Figure 16 24V Input, -15V/1.5A Output

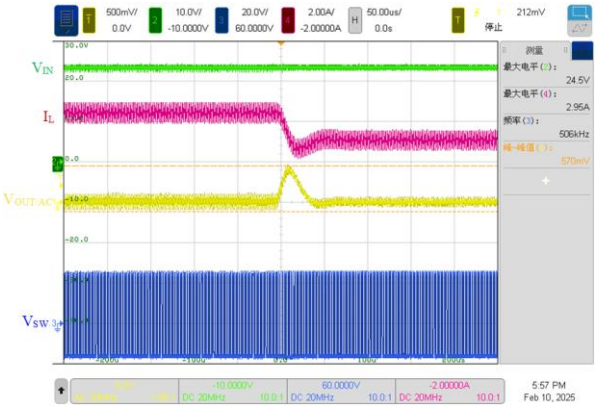


Figure 17 V_{IN} = 24V, -V_{OUT} = -15V, I_{OUT} from 1.5A to 0.7A

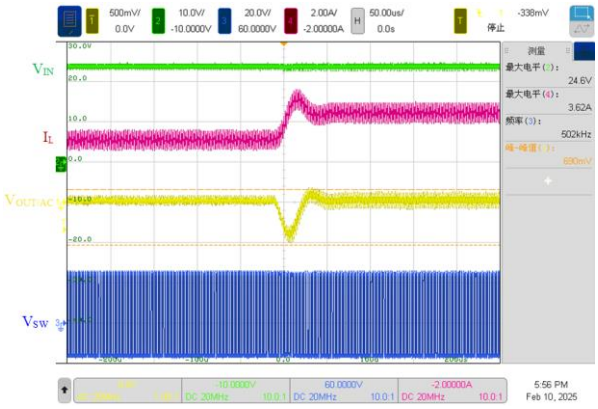


Figure 18 V_{IN} = 24V, -V_{OUT} = -15V, I_{OUT} from 0.7A to 1.5A

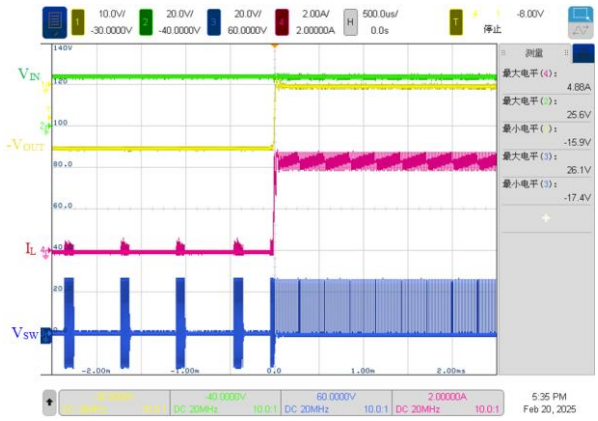


Figure 19 V_{IN} = 24V, -15V/0A Output, SCP Entry

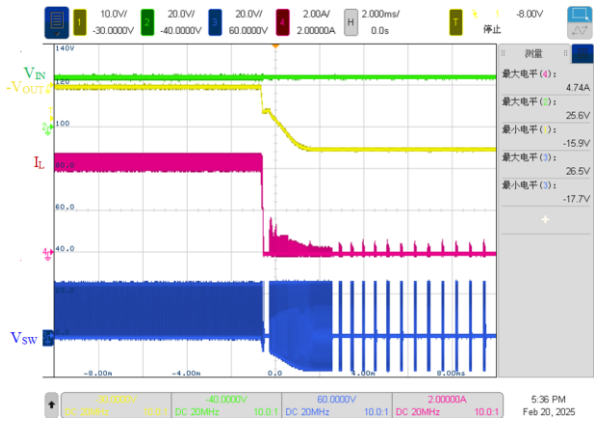


Figure 20 V_{IN} = 24V, -15V/0A Output, SCP Recovery

5 Conclusion

Reconfiguring a Buck converter into an inverting Buck-Boost converter requires the following steps:

1) Calculate the maximum voltage on the converter: V_{IN} + V_{OUT}.
2) Use Table 1 to calculate the maximum inductor current.
3) Select an appropriate Buck IC (meeting the voltage and current stress requirements).
4) Refer to the datasheet to determine component values such as the frequency-setting resistor and feedback divider resistors.
5) Evaluate whether additional designs such as auxiliary circuits or level-shifting circuits are required.
6) For preliminary verification, establish connections on the existing Buck Demo board according to Figure 12:
   a) Redefine the positive output terminal of the Buck circuit as system ground;
   b) Use the IC GND node of the Buck circuit as the negative output terminal;
   c) Keep the input positive terminal unchanged.
7) Special attention should be paid during implementation:
   a) Optimize the layout of input/output capacitors;
   b) Ensure the quality of the feedback (FB) signal path;
   c) Keep the SW node traces as short as possible and away from sensitive signal paths.

6 References

[1] SG Micro Corp. SGM61630 Demo Board Test Report [EB/OL]. https://www.sg-micro.com/evm-detail/EVKIT-SGM61630.

[2] SG Micro Corp. SGM61630 Datasheet [EB/OL]. (2023-12). https://www.sg-micro.com/rect/assets/2e4aa3c1-fd17-4b20-ac75-892cfe5f2e56/SGM61630.pdf.

7 Appendix

Symbol	Description	Value	Unit
C_{IN}	Input Capacitor	8.6	μF
C_{IO}	Input-Output Capacitor	0.1(Recommended)	μF
C_j	Zener Diode Junction Capacitor	>1000	pF
C_{OUT}	Output Capacitor	Calculated	F
D	Converter Duty Cycle	Calculated	--
F_{RHPZ}	Right-Half-Plane Zero Frequency	Calculated	Hz
F_{SW}	Switching Frequency	490	kHz
$I_{L(avg)}$	Average Inductor Current	Calculated	A
$I_{L(peak)}$	Inductor Peak Current	Calculated	A
I_{LIMT}	Current Limit	Minimum Value 3.5	A
I_{OUT}	Output Current	1.5	A
L	Inductance	Calculated	H
Q_G	Gate Charge	--	nC
R_L	Load Resistance	10	Ω
t_{delay}	Delay Time	Calculated	s
V_{ENH}	Enable Input High Threshold	1.17	V
V_{ENL}	Enable Input Low Threshold	1.12	V
V_{GD}	Gate-Drain Voltage	--	V
V_{GS}	Gate-Source Voltage	--	V
V_{IN}	Input Voltage	24	V
V_{OUT}	Output Voltage	15	V
V_{START}	Turn-On Voltage	Calculated	V
V_{STOP}	Turn-Off Voltage	Calculated	V
V_{SYNC_L}	SYNC Input Low Threshold	0.3	V
V_Z	Zener Diode Voltage	4.3	V

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from those in the current version.

Date	Rev	Description
2026-04-17	REV.A	Initial Release

DISCLAIMERS

Where this document mentions specific product models of our company, SGMICRO reserves the right to change circuit design, product specifications and product descriptions without prior notice.

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www.sg-micro.com

CONTACTS

SG Micro Corp
87 Xisanhuan North Road, the IFEC Building, D-11/F,
Haidian District, 100089 Beijing
Tel: 86-10-8882 5716/8882 5717

Shenzhen Office
6 Gaoxin South 6th Road, the Microport Building, 15/F,
Nanshan District, 518063 Shenzhen
Tel: 86-755-2671 5323

Shanghai Office
88 Caoxi North Road, the Charity Building, Room-1706,
Xuhui District, 200030 Shanghai
Tel: 86-21-6439 6434