APPLICATION NOTE
ANE202604002

SGM41570 Series
Laptop Charging Application Design and System Efficiency Estimation

Author: Anchor Wang
Corresponding Author: Cherry Cheng
Reviewers: Iris Liu, Mhofy Tian

SG Micro Corp

April 27, 2026

TRADEMARKS

SGMICRO is a trademark of SG Micro Corp. All trademarks in this document are the property of their respective owners.

Copyright © 2026 SG Micro Corp. All rights reserved.
Without the prior written permission of SGMICRO, any entity or individual shall not extract, copy or adapt part or all of the content of this document.
For more information about SGMICRO, please visit our website at www.sg-micro.com.

ABSTRACT

With the widespread adoption of USB Type-C interfaces and USB Power Delivery (PD) technology in personal electronic devices, the USB Type-C interface has become the mainstream charging port for laptops. Battery charger chips play a critical role in battery charging applications. This document starts with the concept of USB Type-C, first understanding its power delivery connection. Then, focusing on the SGM41570 series Buck-Boost NVDC battery charger chip introduced by SG Micro Corp, it elaborates on the peripheral circuit design for laptop charging applications. It also evaluates the losses at full system load and finally presents the loss distribution in a pie chart. This allows designers to intuitively assess whether the design losses meet requirements based on the proportion of each loss component, thereby optimizing the design.

CONTENTS

1 USB Type-C Overview 2
2 SGM41570 Series Introduction 2
3 Laptop Application Design 3
3.1 Design Requirements 3
3.2 Battery Configuration 4
3.3 External Current Limit Setting 4
3.4 Input Filter Design 4
3.5 Inductor Selection 4
3.6 Input Capacitor Selection 5
3.7 Output Capacitor Selection 6
3.8 Power MOSFET Selection 6
4 Loss Calculation 7
4.1 MOSFET Losses 7
4.1.1 Conduction Losses 7
4.1.2 Switching Losses 7
4.2 Inductor Loss 10
4.3 IC Quiescent Loss 10
4.4 Other Losses 10
4.5 Summary 10
5 References 13
6 Appendix 14

1 USB Type-C Overview

USB Type-C is a revolutionary interface technology that has fundamentally changed the way laptops and other digital devices connect, thanks to its slim design, reversible plug orientation, powerful data transfer and power delivery capabilities. In laptop applications, USB Type-C not only simplifies connector specifications and unifies data cables but also, by integrating USB PD technology, supports power delivery up to 240W[1]. This enables fast and efficient laptop battery charging, significantly shortening charge times. It also allows laptops to meet charging, data transfer, and video output needs simultaneously with a single, lightweight Type-C cable in a wider range of scenarios, greatly enhancing user mobility and experience. Furthermore, the bidirectional charging capability of the Type-C interface means a laptop can also act as a power source for other devices when necessary, increasing flexibility and practicality.

A typical USB Type-C power delivery connection[2] is shown in Figure 1. It mainly consists of three major components: a USB PD controller, a battery charger, and a battery gauge. These components work together through complex logic and control strategies to achieve efficient and safe power transfer, as well as data communication.

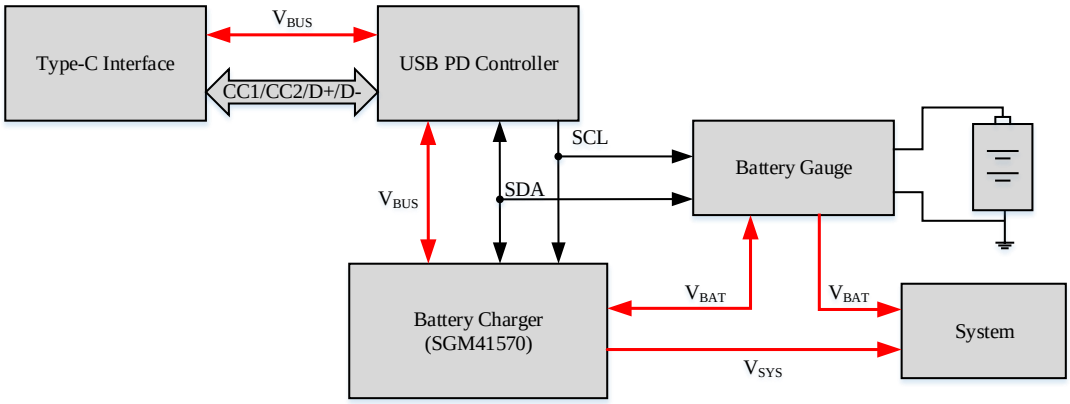


Figure 1 USB Type-C Power Delivery Connection[1]

2 SGM41570 Series Introduction

The SGM41570 series includes two chips: the SGM41570[3] supporting the SMBus interface and the SGM41573[4] supporting the I²C interface. These are powerful synchronous Buck-Boost lithium battery charging controllers, specifically designed for applications requiring efficient charging and power path management, such as laptops and robot vacuums. They support charging 1-cell to 4-cell lithium batteries and integrate various advanced features to meet diverse charging requirements.

First, the SGM41570 offers broad input source compatibility, capable of handling inputs from traditional adapters, USB adapters, and high-voltage USB PD sources. Based on the actual status of the input source and battery, the controller automatically switches to Buck, Boost, or Buck-Boost mode during power-up without host control intervention, ensuring efficient and safe charging.

Second, the SGM41570 features Narrow Voltage DC (NVDC) charging path management and Dynamic Power Management (DPM). These functions optimize power distribution and improve charging efficiency.

[1] V_{BUS} in the figure corresponds to V_{IN} in the following text, and V_{SYS} corresponds to V_{OUT}.

Additionally, the chip supports USB On-The-Go (OTG) mode, allowing it to power peripherals when needed, further expanding application scenarios.

When there is no external load on the USB OTG port, the SGM41570 supports V_{MIN} Active Protection (VAP), preventing system voltage from dropping when system power demand is high. The chip can also monitor adapter current, battery current, and system power. When system power exceeds the available power from the adapter and battery, it issues a flexibly programmable nPROCHOT pulse to notify the CPU to throttle, preventing overload and damage.

In summary, the SGM41570 is a lithium battery charging controller integrating high-efficiency charging, intelligent power path management, broad input source compatibility, and comprehensive protection features, providing an ideal solution for various applications requiring lithium battery charging.

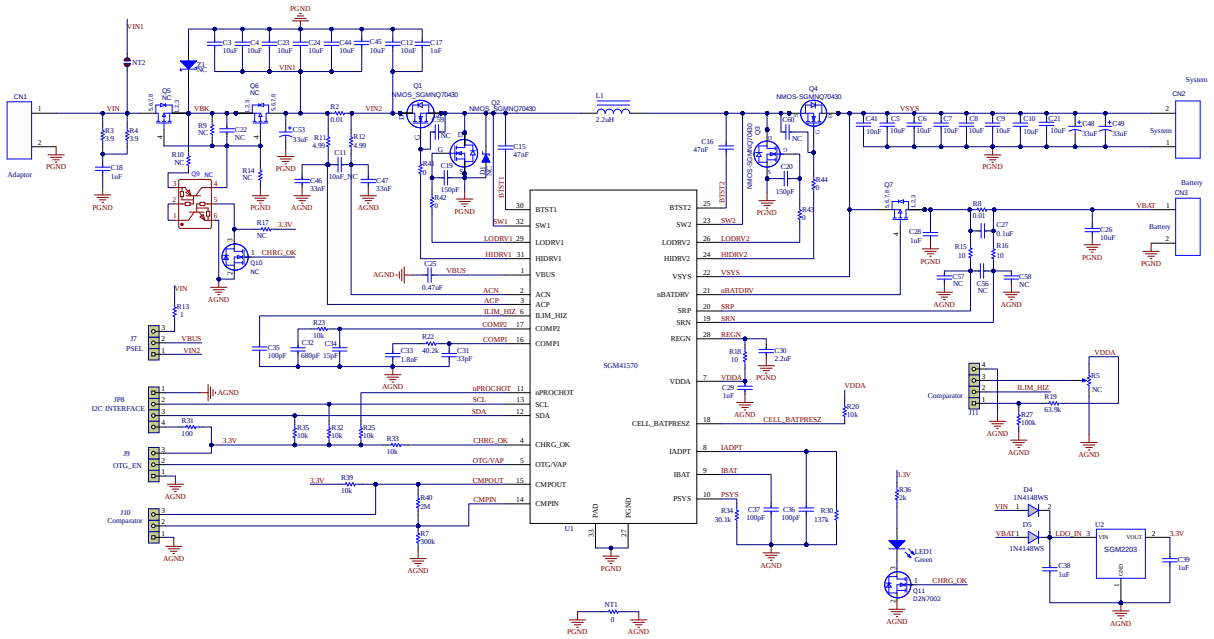


Figure 2 Typical Application Design Schematic

3 Laptop Application Design

In laptop application designs, a Buck-Boost charging controller provides more flexible power adapter capability and more efficient power management. This section uses the SGM41570 Buck-Boost battery charging controller for a laptop application design based on a maximum 20V adapter voltage, 4-cell battery, and 100W peak system power consumption. This reference design achieves a peak efficiency of 96.7% at 100W system power.

3.1 Design Requirements

Parameter	Specification
Input Voltage, V_{IN}	3.6V to 20V, 20V typical
Output Voltage, V_{OUT}	12.3V to 16.8V, 15.2V typical
Maximum System Output Power, P_{OUT}	100W

3.2 Battery Configuration

After the internal LDO is activated, the battery cell count configuration is checked via the bias voltage on the CELL_BATPRESZ pin. For a 4-cell configuration, the CELL_BATPRESZ pin can be pulled up to VDDA through a 10kΩ resistor. Refer to the SGM41570 datasheet[3] for battery configuration thresholds.

3.3 External Current Limit Setting

Connect the ILIM_HIZ pin to a resistor divider between REGN and GND. The target input current limit I_{DPM} can be set using the following formula:

$$V_{ILIM_HIZ} = 1V + 40 \times I_{DPM} \times R_{AC} \quad (1)$$

According to the design requirements, the maximum output power is 100W. Under nominal input voltage conditions, the corresponding input current is 5A. Using a 1.2x input current margin, 6A is set as the input current limit. Selecting a 10mΩ sense resistor, V_{ILIM_HIZ} is calculated to be 3.4V. Based on a 5.6V REGN, choose a 63.9kΩ top divider resistor and a 100kΩ bottom divider resistor.

3.4 Input Filter Design

The SGM41570 uses average current mode control. It detects the input current via the differential voltage between ACP and ACN and reconstructs the inductor current information based on this input current. However, parasitic inductance from the PCB layout can cause high-frequency ringing between ACP and ACN, distorting the inductor current sense signal. This affects the average current control loop and can even lead to output oscillation. Furthermore, distortion in input current sensing degrades the accuracy of the IINDPM loop and IIN_ADC. Refer to the SGM41570 datasheet[3] for functional descriptions of IINDPM and IIN_ADC.

For practical application designs, it is recommended to use the RC filter circuit shown in Figure 3 to filter high-frequency noise caused by PCB parasitic parameters. Design the RC filter time constant between 47ns and 200ns to effectively filter high-frequency noise in the output current sense signal. Setting the RC filter time constant too high is not recommended. Otherwise, in forward Buck mode with discontinuous input current, the distortion in input current sensing will prevent the chip from accurately reconstructing the inductor current information.

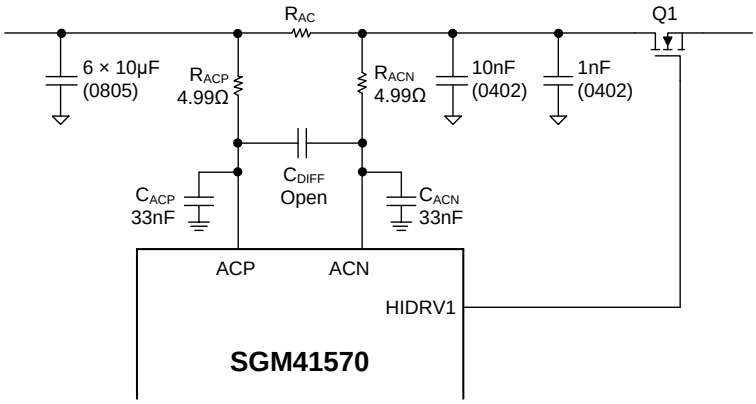


Figure 3 ACN-ACP Input Filter

3.5 Inductor Selection

The SGM41570 offers two switching frequencies: 800kHz and 1200kHz. Higher switching frequencies allow

the use of smaller inductance values and smaller input/output capacitors but increase power MOSFET switching losses. This design uses the default 800kHz switching frequency. Refer to the appendix for the meaning and values of parameters in the formulas below. The inductor saturation current I_{SAT} should be greater than the maximum output current I_{OUT_MAX} plus half the inductor current ripple I_{RIPPLE}:

$$I_{SAT} > I_{OUT_MAX} + \frac{1}{2} \times I_{RIPPLE} \quad (2)$$

In Buck CCM mode ($D = V_{OUT} / V_{IN}$), the inductor current ripple I_{RIPPLE} is given by:

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{f_{SW} \times L} \quad (3)$$

According to the formula above, the maximum inductor current ripple occurs when D = 0.5. When D > 0.5, keeping the input voltage constant, the ripple gradually decreases as the output voltage increases. Based on the design specification range, the maximum inductor current ripple corresponds to V_{IN} = 20V, V_{OUT} = 12.3V.

Typically, inductor ripple is designed to be 20% to 40% of the maximum output current. Taking the ripple factor K_{IND} as 30%, the design inductance value can be obtained using the following formula:

$$L = \frac{V_{IN_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN_MAX} \times f_{SW}} \approx 2.4\mu H \quad (4)$$

Select an inductor with a nominal value of 2.2μH and a saturation current greater than 9.3A. The Wurth 74437356022 inductor meets the design requirements: I_R = 8.5A, $I_{SAT,10\%}$ = 10A, DCR = 13.6mΩ.

3.6 Input Capacitor Selection

Selecting appropriate input capacitors is crucial for absorbing input switching current ripple and minimizing input voltage ripple. The RMS current through the input capacitor can be calculated using formula (5), and the ripple voltage across the input capacitor using formula (6):

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (5)$$

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (6)$$

X7R or X5R ceramic capacitors are generally preferred for input decoupling. Placing a (10nF + 1nF) capacitor combination between the input sense resistor R_{AC} and the power MOSFET Q1 effectively filters high-frequency ringing generated during MOSFET switching.

Based on the design specification range, choose V_{IN} = 20V and V_{OUT} = 15.2V as typical calculation parameters; subsequent calculations will be based on these conditions. Using a 1% input voltage ripple factor in formula (6) yields a minimum input capacitance of approximately 7.5μF. Considering the DC bias effect of ceramic capacitors, select six 25V 10μF 0805 package ceramic capacitors to achieve the required effective capacitance. Refer to the respective manufacturer's datasheet for the DC bias derating curve. To mitigate the impact of extreme conditions like temperature variation and input voltage fluctuation on the effective input capacitance, adding one 25V to 35V, 10μF tantalum capacitor (POSCAP) is recommended.

3.7 Output Capacitor Selection

Selecting appropriate output capacitors is crucial for absorbing inductor current ripple, minimizing output voltage ripple during steady-state and load transients, and ensuring system stability. The RMS current through the output capacitor can be calculated using formula (7), and the ripple voltage across the output capacitor using formula (8):

$$I_{COUT_RMS} = \frac{I_{RIPPLE}}{2\times\sqrt{3}} \quad (7)$$

$$\Delta V_{OUT} = \frac{I_{RIPPLE}}{8\times f_{SW}\times C_{OUT}} \quad (8)$$

Furthermore, formula (9) can be used to calculate the minimum output capacitance. The capacitor should supply energy for at least two switching cycles of current step (ΔI_{OUT}) before the control loop responds to the load change, with a maximum allowable output transient voltage change of ΔV_{OUT} (overshoot or undershoot).

$$C_{OUT} > \frac{2\times\Delta I_{OUT}}{f_{SW}\times\Delta V_{OUT}} \quad (9)$$

Considering a load transient from 10% to 100% and a maximum 5% transient voltage change, the minimum output capacitance is calculated to be approximately 19.5μF. Considering the DC bias effect of ceramic capacitors, select seven 25V 10μF 0805 package ceramic capacitors to achieve the required effective capacitance. Similarly, to mitigate the impact of extreme conditions, adding two 25V to 35V, 33μF tantalum capacitors (POSCAP) is recommended.

3.8 Power MOSFET Selection

The SGM41570 is a Buck-Boost charge management controller requiring external power MOSFETs. It requires four N-channel MOSFETs. The internal gate drivers provide a 5.6V drive voltage. Select MOSFETs with a voltage rating of 30V or higher to meet the 20V input voltage requirement.

The peak inductor current was calculated in Section 3.5. For the actual MOSFET selection, consider a margin of more than 2x for the continuous drain current; I_D should be greater than 18.6A.

To balance conduction loss and switching loss, a commonly used parameter is the MOSFET's Figure of Merit (FOM)[5]. FOM can be calculated using formula (10), where $R_{DS(ON)}$ is the on-resistance and Q_{GD} is the gate-drain charge. A lower FOM value indicates lower total MOSFET losses.

$$FOM = R_{DS(ON)} \times Q_{GD} \quad (10)$$

Generally, for MOSFETs from the same series of a given manufacturer, the FOM value does not vary significantly. After selecting a specific MOSFET series, choose the appropriate MOSFET by comprehensively considering conduction loss, switching loss, and cost. For this design, the SGMNQ70430 N-channel MOSFET is chosen for the four main power switches. It has a voltage rating of 30V and a continuous drain current of 46A.

4 Loss Calculation

The previous chapter detailed the peripheral circuit design. This chapter evaluates the losses at full load based on this design (20V typical input voltage, 15.2V typical output voltage, 100W system output power, 800kHz switching frequency). Finally, the loss distribution is presented in a pie chart. Designers can clearly see the proportion of each loss component from the pie chart, allowing them to assess whether the design losses meet requirements, identify areas for improvement, and optimize the design.

4.1 MOSFET Losses

In this application, the converter primarily operates in synchronous Buck mode. MOSFET-related power losses mainly consist of conduction losses and switching losses. Conduction losses are the sum of the conduction losses of the high-side Q1 and low-side Q2, and are independent of switching frequency. Switching losses include Q1 switching loss, Q2 switching loss, gate drive loss, Q2 body diode loss, reverse recovery loss, and MOSFET output capacitance loss[6].

4.1.1 Conduction Losses

Conduction losses are determined by the MOSFET's on-resistance and the RMS current flowing through it. They can be calculated using the following formulas:

$$P_{COND(Q1)} = D \times I_{L_RMS}^2 \times R_{DS(ON)_Q1} \tag{11}$$

$$P_{COND(Q2)} = ((1-D) - \frac{T_{DEAD_RISE}+T_{DEAD_FALL}}{T_S}) \times I_{L_RMS}^2 \times R_{DS(ON)_Q2} \tag{12}$$

$$I_{L_RMS}^2 = I_{OUT}^2 + \frac{1}{12} \times I_{RIPPLE}^2 \tag{13}$$

Using the above formulas, the calculated Q1 conduction loss is 0.234W, and Q2 conduction loss is 0.065W.

4.1.2 Switching Losses

1. Overlap Losses

During MOSFET switching, both turn-on and turn-off require finite time. During these transition periods, the Q1 MOSFET simultaneously withstands high voltage and current, causing switching loss. The figure below shows the gate-source voltage V_{GS}, drain-source voltage V_{DS}, and drain current I_D waveforms during the Q1 turn-on phase.

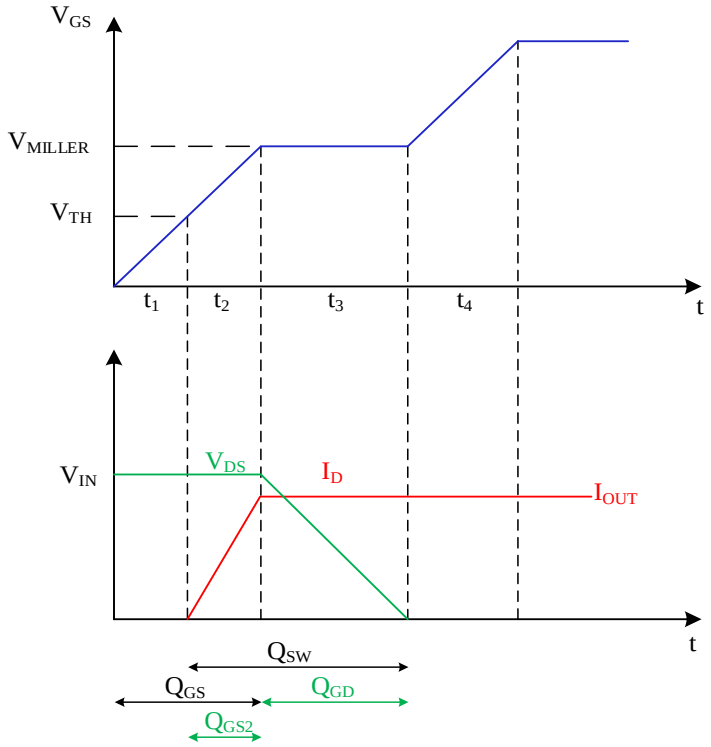


Figure 4 Voltage and Current Waveforms During Q1 Turn-On Phase

The MOSFET turn-on time is calculated as follows:

$$t_{ON} = t_2 + t_3 \tag{14}$$

Wherein $t_2 = \frac{Q_{GS2}}{I_{G2}}$, $t_3 = \frac{Q_{GD}}{I_{G3}}$, $Q_{GS2} = Q_{GS} - Q_{GS(TH)} \approx 0.5 \times Q_{GS}$.

The drive current is estimated using the following formulas[7]:

$$I_{G2_ON} = \frac{V_{REGN} - 0.5 \times (V_{TH} + V_{MILLER})}{R_{ON} + R_G} \tag{15}$$

$$I_{G3_ON} = \frac{V_{REGN} - V_{MILLER}}{R_{ON} + R_G} \tag{16}$$

Wherein $V_{MILLER} = V_{TH} + \frac{2 \times I_{OUT}}{g_{FS}}$, $g_{FS} = \sqrt{\frac{g_{FS_SPEC}^2}{I_{D_SPEC}} \times I_{OUT}}$.

The calculation process for MOSFET turn-off time is similar to turn-on. The drive current formulas for turn-off are:

$$I_{G2_OFF} = \frac{0.5 \times (V_{TH} + V_{MILLER})}{R_{OFF} + R_G} \tag{17}$$

$$I_{G3_OFF} = \frac{V_{MILLER}}{R_{OFF} + R_G} \tag{18}$$

Based on the above formulas, estimated values are t_{ON} = 10.4ns and t_{OFF} = 6.8ns. It is recommended to select MOSFETs with a turn-on time of less than 20ns to reduce the switching loss proportion. Generally, MOSFETs with C_{ISS} less than 1000pF are recommended.

The MOSFET turn-on and turn-off loss calculation formulas are as follows:

$$P_{SW(Q1_ON)} = 0.5 \times V_{IN} \times (I_{OUT} - \frac{I_{RIPPLE}}{2}) \times f_{SW} \times t_{ON} \quad (19)$$

$$P_{SW(Q1_OFF)} = 0.5 \times V_{IN} \times (I_{OUT} + \frac{I_{RIPPLE}}{2}) \times f_{SW} \times t_{OFF} \quad (20)$$

The calculated overlap loss during the turn-on phase is 0.463W, and during the turn-off phase is 0.415W.

2. Gate Drive Loss

The MOSFET gate drive loss is calculated as follows:

$$P_{GATE(Q1)} = V_{OUT} \times Q_G \times f_{SW} \quad (21)$$

$$P_{GATE(Q2)} = V_{OUT} \times (Q_G - Q_{GD}) \times f_{SW} \quad (22)$$

During the low-side MOSFET turn-on process, due to body diode freewheeling, the V_{DS} voltage is already near 0V, so the Miller effect is neglected. The voltage used for loss calculation is V_{OUT} rather than V_{REGN}. Because the chip is operating in Buck mode, the V_{REGN} voltage is generated from V_{OUT} via an LDO. Calculating based on V_{OUT} includes the LDO loss during the driving process. Increasing drive resistance to slow down switching is not recommended. Instead, increasing gate-source capacitance, adding series resistance to the bootstrap capacitor, or adding an RC snubber can be used to slow down MOSFET switching speed. Using the above formulas, the total drive loss for Q1 and Q2 is calculated to be 0.146W.

3. Dead-Time Loss

To prevent Q1 and Q2 from conducting simultaneously and shorting V_{IN}, the converter incorporates two brief dead-time intervals: the rising edge dead-time between Q2 turn-off and Q1 turn-on, and the falling edge dead-time between Q1 turn-off and Q2 turn-on. During these two dead-time intervals, both Q1 and Q2 are off, and Q2's body diode conducts freewheeling current. This introduces dead-time loss (body diode conduction loss) and body diode reverse recovery loss. The dead-time loss is calculated as follows:

$$P_{DEAD} = V_F \times ((I_{OUT} - \frac{I_{RIPPLE}}{2}) \times t_{DEAD_RISE} + (I_{OUT} + \frac{I_{RIPPLE}}{2}) \times t_{DEAD_FALL}) \times f_{SW} \quad (23)$$

The calculated dead-time loss is 0.169W.

4. Body Diode Reverse Recovery Loss

The body diode reverse recovery loss is calculated as follows[8]:

$$P_{RR_Q2} = V_{IN} \times Q_{RR} \times f_{SW} \quad (24)$$

The calculated body diode reverse recovery loss is 0.144W.

5. Output Capacitance Loss

Another power loss associated with MOSFET is the output capacitance loss, caused by charging and discharging the output capacitance C_{OSS}. The calculation formulas are:

$$P_{QOSS_Q1} = 0.5 \times V_{IN} \times Q_{OSS} \times f_{SW} \quad (25)$$

$$P_{QOSS_Q2} = 0.5 \times V_{IN} \times Q_{OSS} \times f_{SW} \quad (26)$$

If the Q_{OSS} parameter is not provided in the MOSFET datasheet, it can be calculated by fitting the provided C_{OSS} vs. V_{DS} curve into a function:

$$P_{COSS_Q1} = f_{SW} \times \int_0^{V_{IN}} C_{OSS}(V_{DS}) \times V_{DS} dV_{DS} \quad (27)$$

$$P_{COSS_Q2} = f_{SW} \times \int_0^{V_{IN}} C_{OSS}(V_{DS}) \times V_{DS} dV_{DS} \quad (28)$$

Since the datasheet for the SGMNQ70430 MOSFET does not provide the Q_{OSS} parameter, the function fitting method is used, resulting in a total output capacitance loss of 0.185W.

4.2 Inductor Loss

Inductor losses mainly consist of winding loss and core loss. Winding loss is composed of DC resistance (DCR) loss and AC resistance (ACR) loss. Core loss includes hysteresis loss, eddy current loss, and residual loss. For the vast majority of inductor manufacturers, the datasheet parameters are insufficient to fully calculate inductor loss. A few inductor manufacturers provide corresponding loss calculation tools to help developers estimate inductor loss. For example, the Wurth website has a loss calculation tool for the 74437356022 inductor. By entering parameters corresponding to the inductor current, the tool generates AC loss and DC loss components. The AC loss result can be used directly, while the DC loss is calculated using the following formula[9]:

$$P_{L_DC} = I_{OUT}^2 \times DCR \quad (29)$$

The calculated inductor DC loss is 0.592W. The AC loss, referenced from the official website calculation, is 0.136W. The total inductor loss is 0.728W.

4.3 IC Quiescent Loss

The SGM41570 control IC itself also has quiescent power dissipation, which can be estimated using formula (30), resulting in an IC quiescent loss of 0.038W.

$$P_{IC} = V_{OUT} \times I_Q \quad (30)$$

4.4 Other Losses

The SGM41570 is a Buck-Boost controller. When the system operates in Buck mode, Q4 is constantly on, and its on-resistance generates corresponding conduction loss. The input current flowing through the 10mΩ sense resistor R_{AC} also generates loss. The respective calculation formulas are:

$$P_{COND(Q4)} = I_{L_RMS}^2 \times R_{DS(ON)_Q4} \quad (31)$$

$$P_{RAC} = D \times I_{L_RMS}^2 \times R_{AC} \quad (32)$$

The calculated Q4 conduction loss is 0.307W, and the sense resistor R_{AC} loss is 0.334W.

4.5 Summary

Based on the loss calculation results in this section, they are summarized in the table below:

MOSFET Losses (W)	Value
Q1 Conduction Loss	0.234
Q2 Conduction Loss	0.065
Turn-on Overlap Loss	0.463
Turn-off Overlap Loss	0.415
Gate Drive Loss	0.146
Dead-time Loss	0.169
Reverse Recovery Loss	0.144
Output Capacitance Loss	0.185
Inductor Losses (W)	
DC Loss	0.592
AC Loss	0.136
IC Quiescent Loss (W)	
Quiescent Loss	0.038
Other Losses (W)	
Q4 Conduction Loss	0.307
Sense Resistor RAC Loss	0.334
Total Loss	**3.228W**

Based on the loss calculation results and the following efficiency formula, the calculated system efficiency for this design is 96.88%.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + P_{LOSS}} \tag{33}$$

Note that the entire calculation process uses parameters at 25℃ and does not consider the impact of system temperature rise. In reality, parameters like the power MOSFET on-resistance and the inductor DCR change significantly with temperature. For a more accurate estimation, the temperature rise effect can be considered, and the results iterated.

Based on the loss table results, the total loss for Q1 and Q2 is 1.82W, with an average loss of 0.91W per MOSFET. Considering the MOSFET thermal resistance, the MOSFET temperature rise can be roughly estimated:

$$t_{RISE} = \frac{P_{Q1} + P_{Q2}}{2} \times R_{\theta JA} \tag{34}$$

According to the formula above, the calculated MOSFET temperature rise is 41.8℃. MOSFET datasheets typically provide a curve of on-resistance $R_{DS(ON)}$ versus temperature. $R_{DS(ON)}$ at the corresponding temperature can be obtained from the temperature rise information. The inductor DCR can be obtained similarly. Recalculating the losses using the temperature-adjusted parameters yields the following results:

MOSFET Losses (W)	Value
Q1 Conduction Loss	0.276
Q2 Conduction Loss	0.076
Turn-on Overlap Loss	0.463
Turn-off Overlap Loss	0.415
Gate Drive Loss	0.146
Dead-time Loss	0.169
Reverse Recovery Loss	0.144
Output Capacitance Loss	0.185
Inductor Losses (W)	
DC Loss	0.700
AC Loss	0.136
IC Quiescent Loss (W)	
Quiescent Loss	0.038
Other Losses (W)	
Q4 Conduction Loss	0.363
Sense Resistor RAC Loss	0.334
Total Loss	**3.445W**

Based on the temperature-corrected loss calculation results, the calculated system efficiency for a 20V adapter voltage, 4-cell battery, and 100W power consumption is 96.68%.

To verify the accuracy of the calculation results, efficiency tests were performed on the SGM41570 DEMO board according to the reference design peripheral circuit[10]:

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)
20.001	5.184	15.201	6.600	96.76

Based on the above data, the difference between the estimated efficiency and the measured efficiency is only 0.08%, which is within a reasonable error range. To clearly and intuitively show the proportion of each loss component, a pie chart of the loss distribution is shown below:

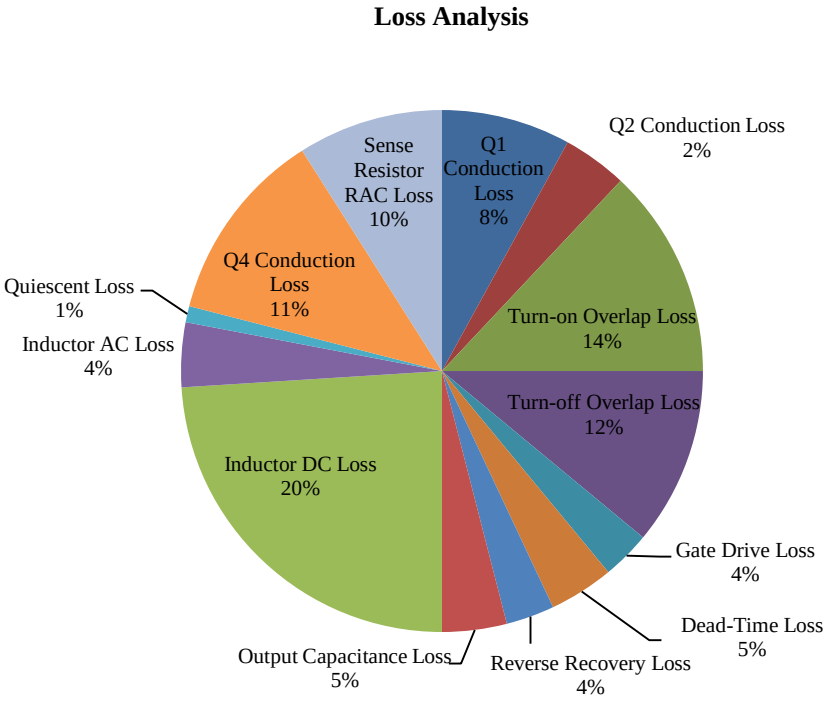


Figure 5 Loss Distribution Pie Chart

5 References

[1] USB 3.0 Promoter Group. Universal Serial Bus Power Delivery Specification [S]. (2022-01).

[2] Texas Instruments Incorporated. Combining Buck-Boost Battery Chargers and USB Type-C Power Delivery for Maximum Power Density [EB/OL]. (2022-05). https://www.ti.com/lit/pdf/SLYY195.

[3] SG Micro Corp. SGM41570 Datasheet [EB/OL]. (2024-04). https://www.sg-micro.com/rect/assets/44ca3412-b7c1-43b8-826b-9dcee8c0b374/SGM41570.pdf

[4] SG Micro Corp. SGM41573 Datasheet [EB/OL]. (2024-04). https://www.sg-micro.com/rect/assets/c877796f-7bf0-4585-87c3-eaa4e6380787/SGM41573.pdf

[5] Utkarsh Jadli, Faisal Mohd-Yasin, Hamid Amini Moghadam, Peyush Pande, Mayank Chaturvedi, Sima Dimitrijev. A Method for Selection of Power MOSFETs to Minimize Power Dissipation [J/OL]. Electronics, 2021, 10, 2150. https://doi.org/10.3390/electronics10172150.

[6] Texas Instruments Incorporated. Power Loss Calculation With Common Source Inductance Consideration for Synchronous Buck Converters [EB/OL]. https://www.ti.com.cn/cn/lit/pdf/slpa009.

[7] The University of Texas at Dallas. Electronic Devices Laboratory Manual [S]. (2013-01).

[8] STMicroelectronics. Calculation of turn-off power losses generated by an ultrafast diode [EB/OL]. (2017-10). https://www.st.com/content/ccc/resource/technical/document/application_note/group0/2b/f3/cc/22/81/d3/4d/89/DM00380483/files/DM00380483.pdf/jcr:content/translations/en.DM00380483.pdf.

[9] Würth Elektronik eiSos GmbH & Co. KG. Accurate Inductor Loss Determination Using Würth Elektronik's REDEXPERT [EB/OL]. (2015-06). https://www.we-online.com/catalog/media/o109035v410%20AppNotes_ANP029_AccurateInductorLossDeterminationUsingRedExpert_EN.pdf.

[10] SG Micro Corp. SGM41570 Demo Board Test Report [EB/OL]. https://www.sg-micro.com/evm-detail/EVKIT-SGM41570.

6 Appendix

Symbol	Description	Value	Unit
C_{OSS}	Q1 or Q2 MOSFET output capacitance	Variable capacitance, varies with V_{DS} voltage	pF
C_{ISS}	Q1 or Q2 MOSFET input capacitance	< 1000	pF
D	Converter duty cycle	Calculated	--
FOM	MOSFET Figure of Merit	--	--
f_{SW}	Switching frequency	800	kHz
g_{FS}	MOSFET forward transconductance	Calculated	S
g_{FS_SPEC}	MOSFET forward transconductance	20 (V_{DS} = 1.5V, I_{D_SPEC} = 15A)	S
I_{CIN_RMS}	Input capacitor RMS current	Calculated	A
I_{COUT_RMS}	Output capacitor RMS current	Calculated	A
I_D	MOSFET drain current	Calculated	A
I_{ON}	MOSFET turn-on gate current	Calculated	A
I_{OFF}	MOSFET turn-off gate current	Calculated	A
I_{OUT}	Converter output current	8.2 (max)	A
I_Q	IC quiescent current	2.5	mA
I_R	Inductor temperature rise current	8.5	A
I_{RIPPLE}	Inductor current peak-to-peak	Calculated	A
I_{SAT}	Inductor saturation current	10	A
I_{L_RMS}	Inductor RMS current	Calculated	A
L	Inductance value	2.2	μH
$P_{COND(Q1)}$	Q1 conduction loss	Calculated	W
$P_{COND(Q2)}$	Q2 conduction loss	Calculated	W
$P_{COND(Q4)}$	Q4 conduction loss	Calculated	W
$P_{COSS(Q1)}$	Q1 output capacitance loss	Calculated from C_{OSS} vs. V_{DS} curve	W
$P_{COSS(Q2)}$	Q2 output capacitance loss	Calculated from C_{OSS} vs. V_{DS} curve	W
PDEAD	Dead-time loss	Calculated	W
P_{GATE_Q1}	Q1 gate drive loss	Calculated	W
P_{GATE_Q2}	Q2 gate drive loss	Calculated	W
P_{IC}	IC quiescent loss	Calculated	W
P_{L_DC}	Inductor DC loss	Calculated	W
$P_{QOSS(Q1)}$	Q1 output capacitance loss	Calculated from Q_{OSS}	W
$P_{QOSS(Q2)}$	Q2 output capacitance loss	Calculated from Q_{OSS}	W
P_{RAC}	Input sense resistor loss	Calculated	W
P_{RR_Q2}	Q2 body diode reverse recovery loss	Calculated	W
$P_{SW(Q1_ON)}$	Q1 turn-on overlap loss	Calculated	W
$P_{SW(Q1_OFF)}$	Q1 turn-off overlap loss	Calculated	W
Q_G	Gate drive charge	8	nC
Q_{GD}	Gate-drain charge	4	nC

Symbol	Description	Value	Unit
Q_{GS}	Gate-source charge	2.2	nC
Q_{OSS}	MOSFET output charge	Calculated from C_{OSS} vs. V_{DS} curve	nC
Q_{RR}	Reverse recovery charge	9	nC
Q_{SW}	MOSFET switching charge	Obtained from datasheet or estimated	nC
$R_{DS(ON)_Q1}$	Q1 on-resistance	7 (V_{TH} = 5.6V, 25℃)	mΩ
$R_{DS(ON)_Q2}$	Q2 on-resistance	7 (V_{TH} = 5.6V, 25℃)	mΩ
$R_{DS(ON)_Q4}$	Q4 on-resistance	7 (V_{TH} = 5.6V, 25℃)	mΩ
R_G	Gate drive resistor	1.3	Ω
R_{ON}	Driver circuit pull-up resistance	5	Ω
R_{OFF}	Driver circuit pull-down resistance	2	Ω
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46	℃/W
t_{DEAD_FALL}	Falling edge dead-time	20	ns
t_{DEAD_RISE}	Rising edge dead-time	20	ns
t_{OFF}	MOSFET turn-off time	Calculated	ns
t_{ON}	MOSFET turn-on time	Calculated	ns
t_{RISE}	MOSFET temperature rise	Calculated	℃
T_S	Switching period	1.25	μs
V_{DS}	Drain-source voltage	--	V
V_F	Body diode forward voltage	0.8	V
V_{GS}	Gate-source voltage	--	V
V_{TH}	Gate-source threshold voltage	1.6	V
V_{REGN}	LDO output voltage	5.6	V
V_{ILIM_HIZ}	ILIM_HIZ pin voltage	Calculated	V
V_{IN}	Converter input voltage	20 (typical)	V
V_{MILLER}	Miller voltage	Calculated	V
V_{OUT}	Converter output voltage	15.2 (typical)	V
ΔV_{IN}	Input capacitor ripple voltage	Calculated	mV
ΔV_{OUT}	Output capacitor ripple voltage	Calculated	mV

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from those in the current version.

Date	Rev	Description
2026-04-27	REV.A	Initial Release

DISCLAIMERS

Where this document mentions specific product models of our company, SGMICRO reserves the right to change circuit design, product specifications and product descriptions without prior notice.

The content of this document is for reference only. All statements, information, and recommendations in this document do not constitute any warranty or commitment. SGMICRO makes no express or implied representations or warranties regarding any errors that may appear in this document, and shall not be liable for any incidental or consequential damages arising from the provision or use of the information contained herein.

This document does not grant any intellectual property license. Except as expressly stated in SGMICRO's product sales terms and conditions, SGMICRO assumes no other liabilities.

www.sg-micro.com

CONTACTS

SG Micro Corp
87 Xisanhuan North Road, the IFEC Building, D-11/F,
Haidian District, 100089 Beijing
Tel: 86-10-8882 5716/8882 5717

Shenzhen Office
6 Gaoxin South 6th Road, the Microport Building, 15/F,
Nanshan District, 518063 Shenzhen
Tel: 86-755-2671 5323

Shanghai Office
88 Caoxi North Road, the Charity Building, Room-1706,
Xuhui District, 200030 Shanghai
Tel: 86-21-6439 6434